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Influence of plasma fluorination on *p*-type channel tin-oxide thin film transistors

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ABSTRACT

This paper describes a high-performance *p*-type tin-oxide (SnO) thin film transistor (TFT) using fluorine plasma treatment on the SnO active channel layer. The influence of fluorine plasma treatment for this *p*-type SnO TFT device was also investigated. Through tuning the fluorine plasma power treated on the SnO active channel layer at low temperature, the optimal *p*-type SnO TFT device exhibits a very high on/off current ratio of 9.6×10^6, a field-effect mobility of 2.13 $cm^2 V^{-1} s^{-1}$, a very low subthreshold swing of 106 mV/dec and an extremely low off-state current of 1 pA at a low driven voltage of <3 V. These good characteristics can be attributed to fluorine plasma treatment on *p*-type SnO channel that reduced crystallized channel roughness and passivated oxygen vacancies and interface traps. This high-performance *p*-type SnO TFT device using fluorine plasma treatment on the active channel shows great promise for future high-resolution and high-speed display applications.

1. Introduction

As compared with the amorphous (α-Si) and polycrystalline silicon (poly-Si) thin film transistors (TFTs) [1–3], the zinc oxide-based (ZnO-based) TFTs [4–10], such as ZnO, Indium-gallium-zinc-oxide (InGaZnO), have attracted much attention for low-cost and large-area display applications in the past few years, which can be attributed to their great advantages, such as high carrier mobility, excellent uniformity, good optical transparency and low temperature processes. However, the ZnO-based TFT devices behave with *n*-type conduction properties and have been demonstrated to obtain high performances. Only a few oxides exhibit *p*-type conduction property with low carrier mobility due to the hole transportation, which is restricted in oxide semiconductors. Therefore, developing the *p*-type oxide TFT devices is of great importance to realize the complementary-metal-oxide-semiconductor (CMOS) devices for applications.

Recently, tin-oxide (SnO) semiconductor materials with high intrinsic mobility show great potential for high driven current and have been demonstrated in *p*-type TFT devices [11–25]. However, due to the high degree of crystallinity of the SnO channel, it is still very challenging for the *p*-type SnO (Sn-rich and O-deficient) TFTs, which have very high off-state current and poor threshold characteristics. Furthermore, since *p*-type SnO channel has higher crystallinity in comparison with O-rich *n*-type SnO, the controllability on process stability and device variation is difficult and needs to be overcome for practical applications.

To solve these issues, we proposed a low-temperature fluorine plasma treatment [26–29] on *p*-type active channel for the *p*-type SnO TFT device and investigated the influence of fluorine plasma treatment by tuning the power of fluorine plasma in this paper. It was reported that the *p*-type conductivity of SnO was mainly attributed to the tin vacancies [30]. In this study, we used the low-power fluorine plasma treatment on the surface of the SnO channel. The fluorine plasma passivated the oxygen vacancies and reduced the hole concentration, resulting in the reduced on-state current but much improved off-state current. The optimal *p*-type SnO TFT device exhibits a very high on/off current ratio (I_{on}/I_{off}) of 9.6×10^6, a field-effect mobility (μ_{FE}) of 2.13 $cm^2 V^{-1} s^{-1}$, a very low

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subthreshold swing (*SS*) of 106 mV/dec, and an extremely low off-state current of 1 pA at a low driven voltage of <3 V. These great enhancements could be ascribed to the fluorine plasma treatment on the *p*-type SnO active channel that reduced crystallized channel roughness and passivated oxygen vacancies and interface traps. These *p*-type SnO TFTs using fluorine plasma treatment on the active channel layer show great potential for next-generation high-performance display applications.

2. Experiments

The top-contact bottom-gate *p*-type SnO TFT devices studied in this work were fabricated using shadow masks in the following processes. First, we used the n^+-type silicon (n^+-Si) substrate as the gate electrode. Next, a 50-nm-thick high-κ HfO_2 dielectric was deposited using electron beam (e-beam) evaporation as the gate dielectric and annealed to initiate the dielectric activation. Subsequently, an 8-nm-thick SnO was formed by physical vapor deposition (PVD) as the active channel layer, followed by a 200 °C annealing. Then, the SnO channel layer was fluorine-plasma-treated using a CF_4 plasma RF unit in a reactive-ion-etching (RIE) system with a pressure of 10 mTorr. The plasma power and time can be varied. Finally, a 50-nm-thick Ni metal was evaporated by e-beam and patterned to form the source and drain (S/D) contact electrodes. For comparison, we also fabricated the SnO TFT device without fluorine plasma treatment on the SnO active channel layer.

The gate stack films of our fabricated *p*-type SnO TFT device were characterized and analyzed using high-resolution transmission electron microscopy (HR-TEM), energy-dispersive x-ray spectroscopy (EDS), x-ray diffraction (XRD), x-ray photoelectron spectroscopy (XPS) and atomic force microscopy (AFM). The measurements of the TFT device characteristics, including current-voltage (*I-V*) property, were performed using HP4156 semiconductor parameter analyzer at room temperature.

3. Results and discussion

Fig. 1(a) shows the HR-TEM image of the gate stack of the fabricated *p*-type SnO TFT device using high-κ HfO_2 as the gate dielectric. Fig. 1(b) shows the fast Fourier-transformation (FFT) image of the SnO active channel layer. From these results, it is obviously observed that the deposited SnO active channel layer has a poly-grain crystalline phase, which indicates that the SnO active channel layer was crystallized during low-temperature 200 °C post deposition annealing (PDA). Fig. 1(c) shows the EDS line profile of the *p*-type SnO TFT device, which indicates the configuration of our device stack and the corporation of F atoms into the *p*-type SnO active channel layer.

To further investigate the different channel properties of the SnO active channel layer with different PDA temperatures, we performed the XRD analysis. Fig. 2(a) and (b) show the XRD spectra of the SnO active channel layer with the PDA treatment at low temperatures of 150 °C and 200 °C, respectively. From the results of the XRD diffraction peaks, it is observed that the metallic Sn atoms and only a small amount of SnO coexist in the SnO active channel layer with the PDA treatment at the temperature of 150 °C. However, with the PDA treatment at the higher temperature of 200 °C, the signal intensity of the SnO significantly increases while that of the metal Sn decreases, which implies that the SnO active channel layer was in mainly crystallized phase and the SnO is the main composition of the active channel layer for the PDA treatment at 200 °C. Thus, the SnO active channel layer with different PDA

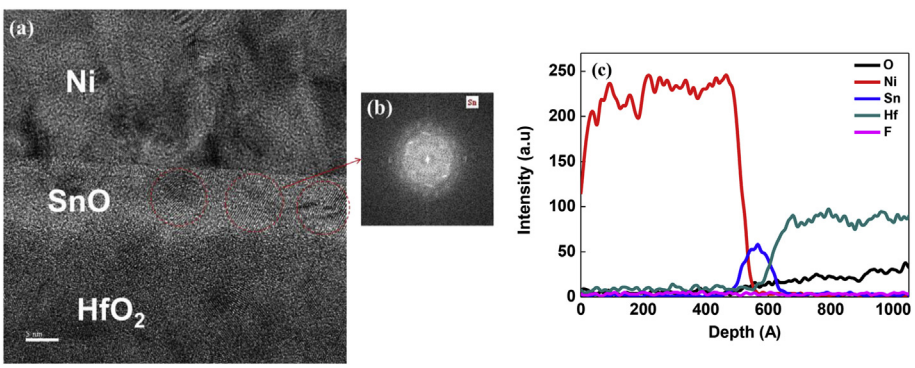

Fig. 1. (a) HR-TEM image of the gate stack of the *p*-type SnO TFT device using high-κ HfO_2 as the gate dielectric, (b) FFT image of the SnO active channel layer for the *p*-type SnO TFT device, and (c) EDS line profile of the *p*-type SnO TFT device using fluorine plasma treatment on the *p*-type SnO active channel layer.

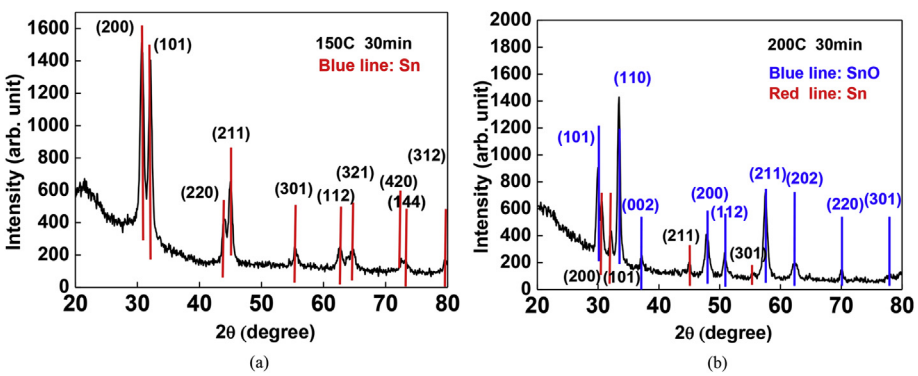

Fig. 2. XRD spectra of the SnO active channel layer with PDA treatment at (a) 150 °C and (b) 200 °C.

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