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Effect of oxide breakdown on RS latches

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Abstract

In this work, the influence of the oxide breakdown on RS latches performance has been analysed. The NAND and NOR RS latch topologies have been compared in terms of noise margin and switching times for different broken down transistors. Moreover, the influence of the additional current path due to BD and of the variation of the MOSFET parameters on the circuit functionality have been separately evaluated. The results show that RS latches do not lose functionality after BD. However, reductions on noise margin and variations on switching times are observed, which depend on the damaged transistor. The performance degradation of the circuit is mainly due to the additional post-BD gate current whereas the variation of the BD MOSFET parameters has only a small influence.

1. Introduction

The impact of dielectric breakdown (BD) on MOS devices and circuits is one of the most critical issues of present CMOS reliability that can limit the IC dimensions reduction. Regarding to this problem, some authors have claimed for a relaxation of the dielectric reliability specifications, showing that even after BD certain digital circuits can still remain functional [1,2]. In order to clarify the problem, further analysis of the dielectric breakdown effect on the circuit performance must be done. In this sense, an accurate description of the post-BD device behaviour, which could be included in circuit simulators, is needed.

At device level, it has been shown that BD not only has associated an additional current through the gate but also a variation of the MOSFET SPICE parameters [3]. However, generally, when studying the circuit reliability, only the BD gate current is considered. In this work, the impact of each of these BD effects on the post-BD functionality of simple digital circuits is analysed. As an example, basic RS latches have been studied, since they are key components of frequency dividers, which are becoming very interesting for RF applications [4]. To perform this analysis, the experimental broken down transistor output characteristics have been modeled and included in a circuit simulator. Noise margin and switching times in two different topologies of RS latches, NAND and NOR RS, have been studied.

2. Experimental

The samples used in this work were nMOSFETs fabricated with 1.5 V bulk technology, SiON as gate dielectric (EOT of 1.6 nm) and draw aspect ratio 350 nm/130 nm. Constant voltage stresses (3 V) were applied to the gate with the other terminals grounded to provoke oxide hard breakdown (HBD). For the considered samples, the similar I_D an I_G currents as a function of the gate voltage (inset of Fig. 1) shows that BD has been produced close to the drain [5]. For the studied circuits (Fig. 3), this case would be the worst one, since for breakdown close to the source in most of the cases, the additional current through the gate would flow to ground, having little influence in the circuit performance. The experimental broken down transistor output characteristics have been described using a model that separately considers the additional BD gate current and the variation of the MOSFET SPICE parameters. In this description, BSIM4 model is combined with a network of

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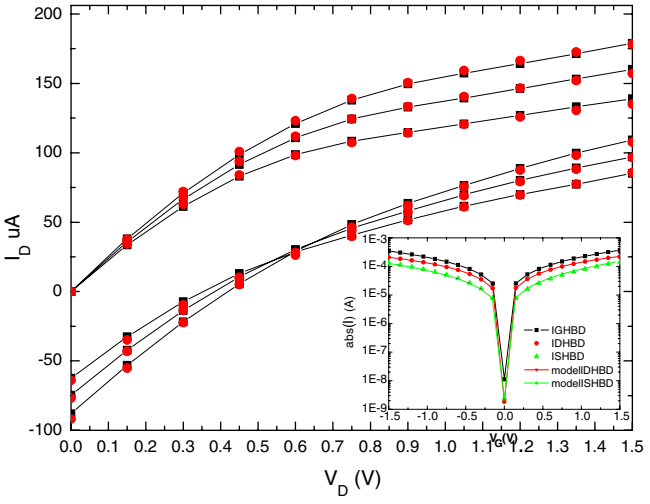

Fig. 1. Experimental I_D–V_{DS} characteristics (symbols) and fittings (continuous lines) for fresh (top curves) and HBD MOSFETs (bottom curves) for $V_G = 1.20$ V, 1.35 V, 1.5 V. Inset: Post-BD currents in all the device terminals vs V_G. These curves show that the HBD path is located close to the drain.

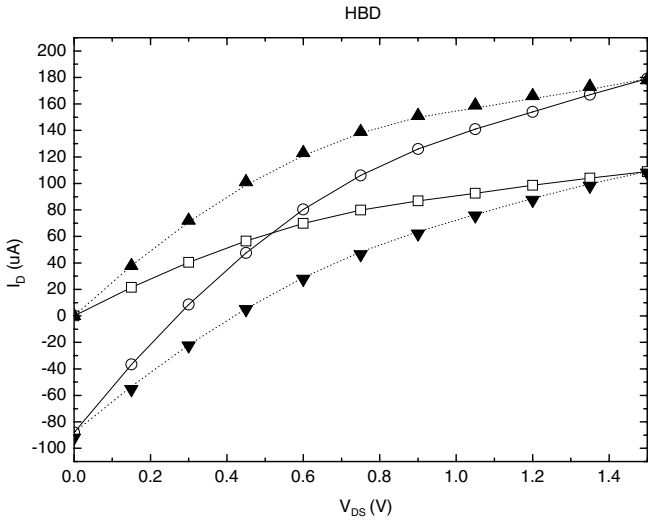

Fig. 2. Experimental I_D–V_D curves measured before BD (up triangles) and after BD (down triangles). The fittings of the curves are shown in dotted lines. Calculated post-BD I_D–V_D curves when only the variation of BSIM4 parameters (open squares) or the BD gate current (open circles) is considered. The gate voltage was 1.5 V in all cases. The BSIM parameters extracted from these curves are used for the simulations shown in Figs. 4 and 6.

diodes and resistances [6] to account for all the BD effects in the post-BD I_D–V_D curves. Fresh and damaged transistor SPICE parameters have been extracted with Aurora software [7] and included in a circuit simulator to observe the influence of oxide HBD on RS latch functionality.

3. Results

I_D–V_{DS} characteristics of the transistors for different gate voltages (V_G) have been measured before and after HBD. Typical curves measured on the devices are shown in Fig. 1 (symbols). After BD, negative values of the I_D current for very low V_{DS} voltages and a decrease of the saturation current due to oxide damage are observed [8]. To fit the experimental data both the BD gate current and the variation of the MOSFET parameters must be considered [3]. Continuous lines in Fig. 1 show these fittings.

The impact of the BD gate current and the variation of MOSFET parameters on the measured post-BD I_D–V_D curves is shown in Fig. 2 for $V_G = 1.5$ V . The experimental I_D–V_D curves measured on fresh and on BD MOSFET have been plotted using up and down triangles, respectively. The BSIM4 model has been used to fit the fresh curves (dotted line). As indicated before, to describe the experimental post-BD I_D–V_D curves (down triangles), BSIM4 model and the contribution of the post-BD I_G to I_D (inset in Fig. 1) are needed (dotted line). The post-BD BSIM4 model parameters are obtained from the I_D–V_G and I_D–V_D curves, once the contribution to I_D of the BD gate current has been subtracted (open squared line). This curve will be used to get the BSIM parameters of case D in Table 1. When only the additional current due to BD is considered (i.e., the post-BD BSIM parameters variations is neglected), the open circles curve in Fig. 2 is obtained (this curve will be used to study case B in Table 1). Note that it is not enough to consider the BD gate current to reproduce the experimental post-BD device behavior. The contribution of the BD gate current to I_D current is considered by adding a network of diodes and resistances connected between gate and drain (since only drain BD is considered in this work) whose values are obtained from the post-BD I_D–V_G curves (inset in Fig. 1).

Table 1
Summary of the four cases simulated to separately evaluate the influence of the BD gate current and the BSIM parameter variation in the degradation of the latch performance

	Without additional BD current	With additional BD current
Fresh BSIM parameters	A	B
Post-BD BSIM parameters	D	C

BD was considered in transistor M3, for NAND and NOR topologies.

To analyse the impact of a drain HBD nMOSFET in the performance of a RS latch, the post-BD MOSFET model has been included in a circuit simulator. NOR and NAND topologies (Fig. 3) have been considered and compared. Additionally, the BD gate current and the variation of the MOSFET parameters have been separately considered. For PMOS devices, the fresh BSIM parameters have been used for all the simulations.

Fig. 4 (middle) shows the NAND RS latch response considering different broken down transistors, for all allowed Reset and Set combinations (Fig. 4 top). Both BD gate current and variation of BSIM4 parameters are simultaneously considered. Differences in the outputs, depending on the broken down transistor (M1, M2, M3