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ScienceDirect
Microelectronics Reliability 47 (2007) 585–592
MICROELECTRONICS RELIABILITY
www.elsevier.com/locate/microrel

Introductory Invited Paper

Silicon nanocrystal non-volatile memory for embedded memory scaling

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Available online 1 March 2007

Abstract

In this paper, we present key features of silicon nanocrystal memory technology. This technology is an attractive candidate for scaling of embedded non-volatile memory (NVM). By replacing a continuous floating gate by electrically isolated silicon nanocrystals embedded in an oxide, this technology mitigates the vulnerability of charge loss through tunnel oxide defects and hence permits tunnel oxide and operating voltage scaling along with accompanied process simplifications. However, going to discrete nanocrystals brings new physical attributes that include the impact of Coulomb blockade or charge confinement, science of formation of nanocrystals of correct size and density and the role of fluctuations, all of which are addressed in this paper using single memory cell and memory array data.

1. Introduction

The scaling of conventional floating gate Flash memories for embedded applications is becoming increasingly difficult primarily because reliability concerns have limited the bottom or tunnel oxide to a thickness of about 10 nm. This in turn manifests in the high peripheral voltages necessary to operate the memory module making embedding this technology inefficient. From a manufacturing viewpoint, there is process complexity associated with embedding this memory with standard CMOS and manifests as about 10 mask adders. Non-volatile memory technology based on discrete silicon nanocrystals has been shown to be immune to oxide defects which arise during program/erase operations and allows reduction of the tunnel oxide thickness and consequently, memory operating voltage [1–3]. Fig. 1 shows a schematic cross section of a nanocrystal memory device with a layer of isolated Si nanocrystals forming the floating gate. Typically the nanocrystals may be between 3 and 10 nm in diameter.

The use of silicon nanocrystals as the charge storage medium has significant benefits over that of nitride in SONOS type memories when operating with hot carrier injection (HCI) for programming and Fowler–Nordheim (FN) tunneling for erase due to the ability to utilize tunnel oxide thickness in the order of 5 nm, which are needed to mitigate read disturb effects. At this tunnel oxide thickness, issues that impact SONOS type memories such as erase saturation [4] shown in Fig. 2 are not present in the nanocrystal-based memory. This erase saturation makes SONOS erase less as the erase voltage or the tunnel oxide thickness is increased. The scaling of the tunnel oxide in nanocrystal memories results in embedded memory modules which can operate with a maximum on chip voltage of 6 V allowing reduction of the memory module size by up to a factor of two [2].

However, the replacement of a floating gate by nanocrystals brings new physical aspects and challenges. Charge confinement effects in nanocrystals can influence device operation and characteristics. Further, optimal device performance requires the formation of nanocrystals of the correct size and density and preserving them during subsequent processing. Since the nanocrystals are not formed by patterning, there is stochasticity in their assembly and hence

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doi:10.1016/j.microrel.2007.01.047

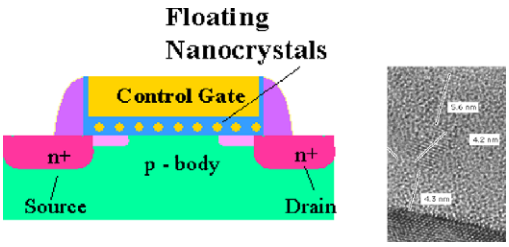

Fig. 1. Nanocrystal memory bit-cell with silicon nanocrystals (~5 nm) overlying a tunnel oxide (4–6 nm).

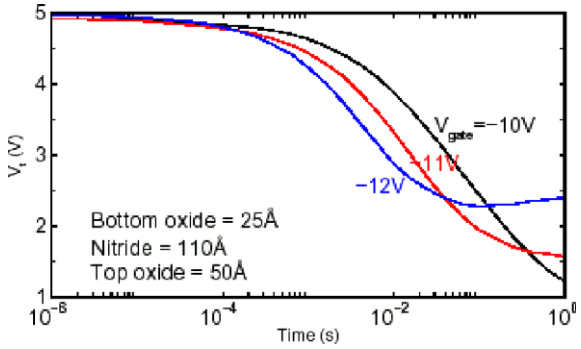

Fig. 2. Erase saturation in SONOS non-volatile memory indicating the reduced memory window as the erase voltage is increased.

fluctuations can become important. In this paper, we discuss the salient aspects of nanocrystal memory for HCI/FN operation.

The outline of this paper is as follows: in Section 2, we discuss the unique features of nanocrystal memory; in Section 3, we review the bit-cell integration emphasizing the deposition of silicon nanocrystals by CVD and their subsequent passivation; in Section 4, we discuss memory bit-cell data characteristics; in Section 5, we discuss the role of nanocrystal fluctuations and in Section 6, we summarize the paper.

2. Charge storage in silicon nanocrystals

In this section, we summarize some of the salient aspects of nanocrystal memory devices such as that shown in Fig. 1. The threshold voltage shift due to electron storage is given by [1] as

$$\Delta V_t = \frac{npq}{\varepsilon_{ox}}\left(t_{control} + \frac{\varepsilon_{ox} t_{nc}}{2\varepsilon_{Si}}\right), \tag{1.1}$$

where n is the nanocrystal number density, p is the average number of electrons stored per nanocrystal, q is the electronic charge, ε represents the medium permittivity, t_{nc} is the nanocrystal diameter and $t_{control}$ represents the control oxide thickness. Clearly, for storing a given number density of electrons, np, susceptibility to isolated defects in the tunnel oxide is mitigated by having a higher density, n, of nanocrystals and minimizing the number, p, of electrons stored per nanocrystal. For nanocrystals to be sufficiently electrically isolated with respect to tunneling transport, their typical separation must be greater than about 4 nm from one another. Having the minimal area fraction of nanocrystals mitigates the probability of defects underlying any nanocrystal. However, charge confinement effects or Coulomb blockade effects to be briefly discussed, increase the energy levels when multiple electrons are stored and this becomes pronounced below a nanocrystal size of about 3 nm. This adversely limits charge retention characteristics and limits the size to be greater than about 4 nm. The raising of energy levels may be approximately computed from the reversible work needed to charge the nanocrystal with the additional electron and may be computed from the self capacitance of the nanocrystal which is given by

$$C = 2\pi\varepsilon_{ox} d. \tag{1.2}$$

The increase in energy for a nanocrystal on addition of the nth electron is given by

$$\Delta E_{n,n-1} = \frac{e^2}{2C}[n(n-1) - (n-1)(n-2)] = \frac{(n-1)e^2}{C}. \tag{1.3}$$

This implies that the electrochemical potential change due to the addition of each electron is given by

$$\Delta\mu = \Delta E_{n,n-1} - \Delta E_{n-1,n-2} = q^2/C. \tag{1.4}$$

Since the self capacitance of nanocrystals in the size range of interest is in atto farads (10^{-18} F) or smaller, this change in energy level is significant. For example, for a 5 nm silicon nanocrystal, the self capacitance is approximately 0.7 atto farads and the above energy level increase is of the order of a few tenths of 1 eV. In a nanocrystal memory, the capacitance of a nanocrystal is higher due to capacitive coupling to other nanocrystals and substrate and the presence of a dielectric medium. As such, the energy level for a 5 electron nanocrystal is about 0.5 eV above ground state. This raising of energy levels adversely impacts tunneling mediated charge loss through the bottom oxide and limits the number of electrons that can be stored. The raising of energy levels, however, facilitates erasure of the memory as it is easier to remove the charges by Fowler–Nordheim injection.

We now contrast the nanocrystal memory characteristics with SONOS type memories. A significant advantage of SONOS type memories is the significantly smaller process complexity compared to forming nanocrystals of correct size and density and preserving them during subsequent processing. However, nanocrystal memory brings device advantages. Deeper electron storage traps (~3 eV) compared to nitride traps (1–2 eV) improve electron retention within the nanocrystal. The ability to physically observe the trap centers and obtain their number density and size somewhat mitigates the process complexity. Further, local field effects as well as Coulomb blockade discussed above are central to superior FN erase characteristics compared to SONOS. This enables the standard HCI–FN NOR archi-