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# Ionising radiation and electrical stress on nanocrystal memory cell array

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**Abstract**

In this work, we have investigated the effects of irradiation and electrical stress of nanocrystal memory cell arrays. Heavy ion irradiation has no or negligible immediate effects on the nanocrystal MOSFET characteristics, and on the programming window of the cells. By electrically stressing irradiated device, we see accelerated oxide breakdown similar to that previously observed on conventional thin gate oxide MOS capacitors, but no appreciable change of the degradation kinetics in terms of programming window closure and shift. The accelerated breakdown is ascribed to the degradation of the oxide–nitride–oxide (ONO) layer used as control oxide after exposure to ionising irradiation.


## 1. Introduction

Nanocrystal memory (NCM) represents the most natural evolution of the flash memory concept, replacing the polysilicon floating gate with an array of discrete dots storing the electric charge [1–3]. Among the most important feature of NCM is the improved immunity to oxide leakage current, such as stress induced leakage current, which is a crucial issue for reliability and scaling of the floating gate memory cell. In fact, the malfunction of one silicon nanocrystal (NC) close to the oxide defect is not critical for data retention, permitting a strong reduction of the effects of structural and/or stress-induced defects in the tunnel oxide.

When considering radiation tolerant components, it can be argued that NCM technology has an intrinsic radiation tolerance to both total ionising dose (TID) effects and single event effects (SEE), due to the ability of the cell to maintain functionality with only a fraction of intact charge storage nodes, in contrast to a monolithic floating gate. In principle, the thin tunnel oxide of irradiated NC cells may exhibit many of the degradation phenomena previously observed in thin gate oxides, such as radiation induced leakage current (RILC) [4], radiation soft breakdown (RSB) [5], accelerated breakdown [6], and the reduction of the MOSFET drain current driving capability [7]. In the last years very few works have addressed these issues, mainly devoted to the evaluation of different cell designs and processes [8,9].

In this work, we focused our attention on the effects of irradiation and electrical stress on NC memory cell arrays. At a first glance heavy ion irradiation has negligible effect on NC cells characteristics immediately after irradiation. On the contrary we show that, by electrically stressing irradiated device, we see accelerated oxide breakdown, even though no appreciable change of the degradation kinetics until breakdown is observed.

## 2. Experimental and devices

Throughout this work, we studied single NCM cells and NCM arrays consisting of 256-kbit cells in parallel connection (Cell Array Stress Test, CAST) provided by ST Microelectronics (Catania, Italy). The aspect ratio of each nanocrystal MOSFET is $W/L = 0.2\ \mu m/0.3\ \mu m$. The tunnel oxide is 5-nm thick and thermally grown on $\langle 100 \rangle$ silicon substrate. The silicon nanocrystal layer was deposited by LPCVD, using standard semiconductor equipments. The external control oxide consists of an oxide–nitride–oxide (ONO) stack with an equivalent oxide thickness

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(EOT) of 12 nm. Silicon nano-islands were realized by low pressure CVD (LPCVD) process in the Si nucleation regime using $SiH_4$ as a precursor. A post-deposition annealing was carried out in order to render crystalline the islands. A nanocrystal density of $5 \times 10^{11}$ cm$^{-2}$ was determined by TEM measurements, with an average nanocrystal diameter of 6 nm.

Irradiation was performed at the SIRAD facility of the Tandem Van Der Graaf accelerator at the Legnaro National Laboratories, Italy [10]. The samples were irradiated with I ions ($E = 301$ MeV, LET = 64 MeV cm$^2$ mg$^{-1}$), Ni ($E = 182$ MeV, LET = 31.3 MeV cm$^2$ mg$^{-1}$) ions at the wafer level. The device terminals were kept floating during irradiation. The number of ion hits on each device was evaluated as the gate area of the irradiated device times the fluence, and as such is affected by some uncertainty. For each ion source we used three ion fluences: $0.83 \times 10^8$ ions/cm$^2$, $1.7 \times 10^8$ ions/cm$^2$, and $3.3 \times 10^8$ ions/cm$^2$, corresponding to an average hit cells percentage per array of 5%, 10% and 20%, respectively. The maximum ion fluence has been chosen in order to keep small enough the percentage of double hits in one cell, still having a statistically significant population of hit cells. We calculated that the double hit probability is 0.12%, 0.45%, 1.6% for an ion fluence of $0.83 \times 10^8$ ions/cm$^2$, $1.7 \times 10^8$ ions/cm$^2$, and $3.3 \times 10^8$ ions/cm$^2$, respectively.

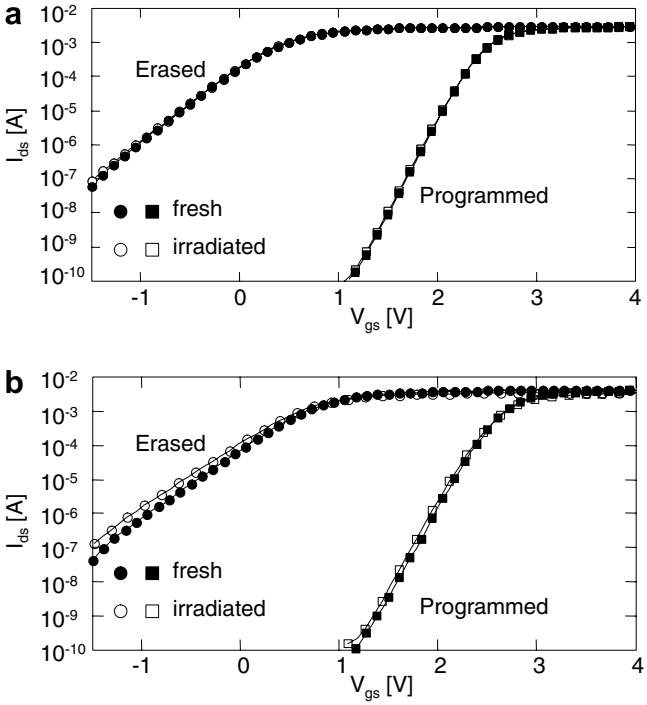


Fig. 1. $I_{ds}$–$V_{gs}$ curves taken before and immediately after the irradiation with Ni-ions (a) and I-ions (b).

## 3. Results

In Fig. 1, we show the $I_{ds}$–$V_{gs}$ characteristics of some CAST arrays irradiated with $3.3 \times 10^8$ I ions/cm$^2$ and $0.8 \times 10^8$ Ni ions/cm$^2$. Immediately after irradiation we generally observe small or negligible variations of either the drain current or the average $V_t$ of the CAST array, even though we cannot exclude small variations in the tail of $V_t$ distribution. The average CAST $V_t$, has been defined as the peak of the cell $V_t$ distribution within the CAST and it was extrapolated by using the method proposed in [11]. In order to assess if any latent damage is present in the tunnel or control oxide even in those samples which do not exhibit any change after irradiation, we submitted to accelerated electrical stress both irradiated and not irradiated array, using different electrical stress techniques:

(a) Constant voltage stress (CVS) with $|V_g| = 15$ V to 18 V.
(b) Bipolar pulsed voltage stress (BPVS) by applying square pulses to the gate between $-V_g$ and $+V_g$ ($V_g = 15$ V or 16 V) and pulse frequency from 10 Hz to 100 kHz.

All stresses were carried out with grounded source, drain and substrate. Figs. 2–4 summarize the effects of electrical stresses on some fresh and irradiated devices by using the two stress methods listed above. The gate current during electrical stress is plotted in Fig. 2, showing the accelerated breakdown of irradiated oxide, at least when CVS is

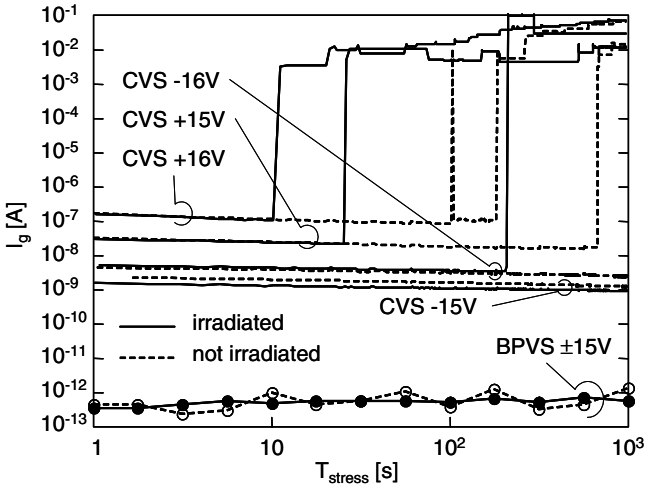


Fig. 2. Gate current during electrical stresses performed on irradiated and not irradiated devices. Different $V_g$ polarities and modes (CVS and BPVS) are compared. For BPVS we show the $I_g$ value read from $I_g$–$V_g$ curves at $V_g = 4$ V.

applied. The (programmed/erased) P/E state $V_t$ evolution is shown in Fig. 3 for CVS and in Fig. 4 during CVS and BPVS. In both figures irradiated and fresh devices are shown. Comparing Figs. 3 and 4 we observe no or negligible $V_t$ variation during negative CVS, while for both fresh and irradiated devices we observe a positive shift of the threshold voltages during positive CVS. In addition, BPVS produces also the progressive thinning of the programming