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Microelectronics Reliability 47 (2007) 815–818
MICROELECTRONICS RELIABILITY
www.elsevier.com/locate/microrel

Total ionizing dose reliability of thin SiO_2 in PowerMOSFET devices

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Available online 22 February 2007

Abstract

This work shows an experimental study on the reliability of PowerMOSFET devices used in satellitar application. The total irradiated dose (TID) tolerance degree of a gate oxide as a function of its thickness and growth process has been investigated. Different oxide thin films, with thickness ranging from 25 nm to 35 nm, integrated in 30 V and 100 V N-channel STM PowerMOSFET vehicles, have been examined. The gate threshold voltage has been used to evaluate the degradation, in comparison to a predictive model. The attention is stressed onto non-ideality factors involving the gate degradation.

1. Introduction

In the last few years STMicroelectronics envisaged the prime objective of building up a number of defined application-oriented technologies for discrete PowerMOSFET devices, with proper hardness against ionizing radiation (photons and energetic particles), mainly targeted to satellitar applications.

Particular attention has been stressed on the Total Irradiated Dose (TID) tolerance. The total dose effects show up as a device degradation that accumulates during operation in the ionizing ambient, until the device performances are strongly modified. In the case of a PowerMOSFET device used in a satellitar application, the only TID mechanism that significantly modifies the device quality and performance is due to the high energy γ photons that impinge the device during its entire life. The effect of such huge irradiation is the massive creation of hole–electron pairs within the dielectric layers and a consequently large positive charging of the same layers, while electrons are promptly conveyed to the gate electrode due to their larger mobility in the oxide. Also a detrimental effect on the dielectric/silicon interfaces may occur, above all when very large photon fluxes and fluences are involved. The most important layer in the operation reliability of the PowerMOSFET is surely the gate dielectric. Therefore, it turns out that a proper study of the process and structure characteristics of such a layer is of great importance in assessing its TID robustness.

In Fig. 1 the traditional model of charge transport and trapping in irradiated thermal SiO_2 is shown. Ionizing radiation creates electron–hole (e–h) pairs in the oxide. When a positive gate-to-substrate bias is applied the created holes, exhibiting a lower effective mobility, drift towards the Si/SiO_2 interface and a large fraction of them are trapped, with the remainder exiting into the Si. As a consequence of these processes, charged hydrogen species (e.g., protons) are liberated in the oxide bulk or near the interface and move to the interface itself, where reactions with passivated dangling bonds can be favored to form interface traps [1].

The charge trapping in the gate oxide and the Si/SiO_2 interface states generation may cause a gate threshold voltage shift or more generally a degradation of the channel parameters.

A first-order model has been applied to evaluate the accumulated dose effects on V_{gsth}, which predicts a linear dependence on the dose and a quadratic dependence on the oxide thickness. The model accounts only for a bulk homogeneous charging with trapped holes, so to assume that the charge centroid is in the middle of the oxide layer. A comparison between the expected gate threshold change,

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doi:10.1016/j.microrel.2007.01.007

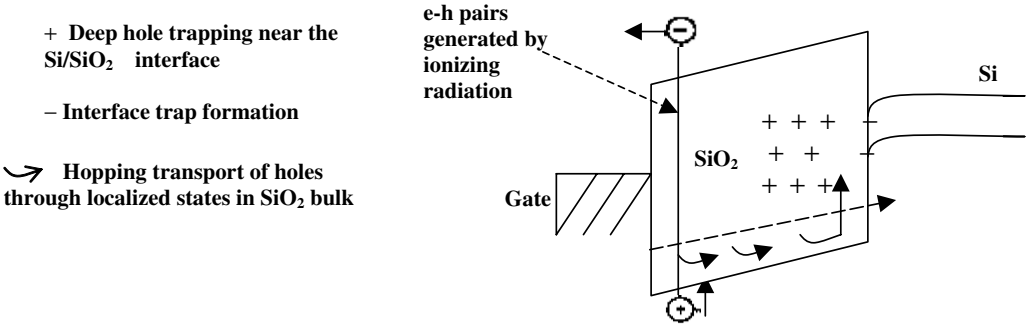

Fig. 1. The charge generation, transport and trapping in a biased oxide layer. The primary effect in sub-micron device is the hole trapping near the Si/SiO_2 interface.

due only to trapping in the oxide bulk, and the observed V_{gsth} change allowed a coarse but significant evaluation of the near-interface influence on the degradation magnitude. An ad-hoc factor f is introduced in the above model to account for the latter non-ideal interfacial contributions, as well as displacement of the trapped holes distribution and hole trapping efficiency.

$$\Delta V_{gsth} = f \cdot \Delta V_{ot} = f \cdot \frac{qgD}{\varepsilon_{ox}} x_{ox}^2 \quad (1)$$

In the above model, $g = 7.2 \times 10^{12}\ \mathrm{rad}^{-1}\ \mathrm{cm}^{-2}$ is the hole generation rate per unit dose in SiO_2, q is the electron charge, D is the accumulated dose in krads, ε_{ox} is the oxide dielectric constant and x_{ox} is the oxide thickness in cm.

The f-factor is a fundamental parameter for relatively modest total doses (max 10^2 krad) and it produces a relatively smaller threshold voltage variation compared to the ideal bulk model ($f = 1$) either in N-channel devices or in P-channel ones.

From Eq. (1) it can be observed that in total dose aging regime the electrical degradation may be minimized in two ways: (1) reducing the gate oxide thickness; (2) reducing the capture probability, that is trap density and /or trapping cross section, of generated holes due to interaction with ionizing radiation.

2. Experimental

The Calliope Cobalt-60 γ-ray source (1.25 MeV) located at the ENEA National laboratories (Rome) was used for irradiation campaigns at low dose rate. The adopted test method is strictly based on ESA-SCC 22900 specification. A test flow block diagram is shown in Fig. 2.

The total irradiation has been divided into five steps: 10, 20, 30, 50, 70 krad, with a two hours maximum interval between one step and the following.

During irradiation process, realized at room temperature and with a dose rate of 0.1 rad/s so to allow a clear separation between dielectric charging and annealing effects, six samples per type have been biased. Three of them have been biased in V_{gss} configuration, at $V_g = 12$ V (Fig. 3a) and the remaining in V_{dss} configuration at 80%

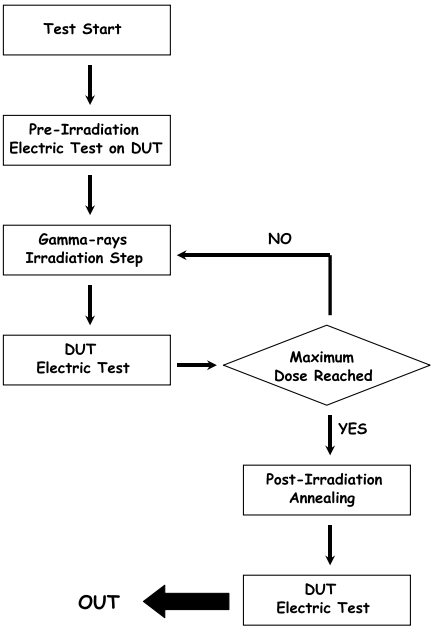

Fig. 2. Block diagram of the test flow used for TID test.

of the nominal blocking voltage (Fig. 3b). In the former case a larger involvement of the SiO_2 near-interface region is expected due to the presence of a transverse field that pushes the holes created within the dielectric layer towards the interface. In the latter case the transverse field is absent so that a uniform trapped hole density within the layer is expected. The seventh sample was left unstressed for referencing. The measurement of in-line electrical parameters, mainly the V_{gsth} threshold voltage and the drain/source leakage and breakdown voltage, has been performed using an HP4155 DIGILAND PARAMETER.

A final 168 h, 100 °C storage (under bias) and following electrical measurement has been performed in each case.

In Fig. 4 the cross section of the STM trading Power-MOSFET used in this experiment is sketched. In particular, we examined a set of gate oxide thin films, with thickness ranging from 25 to 35 nm, integrated in 30 V and 100 V N-channel PowerMOSFET vehicles belonging to three different technology frames, as shown in Table 1.