Journal of Alloys and Compounds 722 (2017) 259–264

Contents lists available at ScienceDirect

Journal of Alloys and Compounds

journal homepage: http://www.elsevier.com/locate/jalcom

Investigation of the barrier properties of copper-vanadium alloys with a sub-tantalum layer on low-k dielectrics

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ARTICLE INFO

Article history:
Received 29 March 2017
Received in revised form
5 June 2017
Accepted 8 June 2017
Available online 13 June 2017

Keywords:
Cu interconnect
Diffusion barrier
Cu-V alloy
Ta
Low-k dielectric

ABSTRACT

In this study, we investigated the effects of a sub-Ta layer on the self-forming barrier process of a Cu-V alloy on low-k dielectrics. To determine how the sub-Ta layer affects the V-based self-forming barrier performance, Cu-V/low-k and Cu-V/Ta/low-k samples were compared using various analysis methods. The thickness, chemical composition, and reliability performance of the V-based interlayer with or without the sub-Ta layer were determined by transmission electron microscopy (TEM), X-ray photoemission spectroscopy (XPS), and thermal stability analysis, respectively. Although the sub-Ta layer adversely affected the decrease of the sheet resistance of the Cu alloy and the formation of a V-based interlayer, the experimental results revealed that the Cu-V/Ta/low-k samples exhibited good reliability and barrier properties, indicating that these properties for a Cu-V barrier layer can be enhanced by introducing a thin Ta sub-layer. XPS analysis showed that the sub-Ta layer affects the formation of a V oxide layer not only by blocking the diffusion of V atoms, but also due to the formation of Ta oxide. In the case of a V-based interlayer with a sub-Ta layer, both Ta_2O_5 and V_2O_5 compounds were formed on the low-k layer. Furthermore, according to the leakage current results, although the introduction of the sub-Ta layer improved the reliability and thermal stability of the self-forming barrier process, the Cu-V/Ta/low-k/Si structures demonstrated increased current densities under the 550 °C thermal stress condition. This indicates that the Cu-V alloy with the sub-Ta layer needs to be further investigated to improve the thermal stability.

1. Introduction

As microelectronic integrated circuits (ICs) continue to decrease in scale, the resistive-capacitance (RC) delay limits the overall speed performance of IC devices. In order to reduce the RC delay, Cu and low-k dielectric systems have been used as the interconnect metal as a replacement for Al and silicon oxide (SiO_2) systems. However, Cu has a high diffusivity in Si (diffusion coefficient, $D = 3 \times 10^{-4}$ cm^2/s) and Si-based dielectrics, where it can impact the function of the active element by creating deep trap states or providing shorter paths in the case of agglomeration [1–5]. Thus, to prevent the diffusion of Cu into a low-k dielectric, a diffusion barrier was introduced in the Cu metallization process. The diffusion barrier must protect the Cu wires to ensure that they are reliable and remain intact for decades under current stress. However, since the width of the Cu interconnect lines decreases to the low submicron scale, an increase of the resistivity of the metal lines remains a challenge in semiconductor manufacturing. One of the primary reasons for the increase in electrical resistivity of Cu interconnect lines is the reduction of the Cu cross-sectional area, causing an increase of the barrier volume fraction in the interconnect lines [6,7]. Under this regime, traditional TaN/Ta combination layers are limited and the reliability of the interconnect has suffered.

To overcome this problem, a “self-forming barrier” process has been introduced. This process involves direct deposition of a Cu alloy thin film on Si-based dielectrics followed by annealing to transport the alloying element to the interface between the Cu alloy and the dielectrics. This forms a thin oxide or silicate layer by reacting with the Si-based dielectric [8–15]. The self-forming barrier is known to enhance the adhesion of the dielectric with the Cu line as well as the electromigration resistance.

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http://dx.doi.org/10.1016/j.jallcom.2017.06.103
0925-8388/

In addition, because of the difference of the barrier interface chemistry from the dense oxide as well as the presence of pores and roughness, there is significant interest in examining the reliability of an ultrathin Cu barrier on low-k materials [16,17]. If a non-stoichiometric metal oxide forms at the interface, it can lead to tremendous current leakage because of the drifting of metal ions into the porous dielectric during thermal annealing. Lee et al. and Miyazaki et al. demonstrated that unstable interfaces are common among porous low-k dielectrics, including transition metals and Cu alloys on silica-based matrixes [18,19].

In our previous reports, we demonstrated that a Cu-V alloy self-formed an excellent diffusion barrier layer on various low-k dielectrics upon annealing and the formation of a barrier at the interface of the Cu alloy and the low-k dielectric was enhanced by UV curing due to the porosity and chemical composition of the dielectric layer [20,21]. However, we observed that the leakage current in the Cu-V alloy/low-k sample without UV curing/Si showed an immediate increase under conditions of no thermal stress. This indicates that the diffusion of Cu into the low-k layer occurred even faster than the formation of the self-forming layer. This phenomenon tends to worsen upon using ultrathin Cu alloy seed layers with a small amount of alloy content. Only a few reports have mentioned the effects of using low-k dielectrics with pore sealing characteristics in the process of barrier self-formation and no published reports have focused on this topic.

In this study, we introduced a sub-Ta layer on the surface of the low-k dielectric to alleviate the immediate Cu diffusion during the barrier formation process. Cu-V/low-k and Cu-V alloy/Ta/low-k samples are proposed and the properties of the barrier at the interface between the alloy films and dielectric substrates were compared. The formation of the interlayer and the chemical compositions were examined using transmission electron microscopy (TEM), Auger electron spectroscopy (AES), and X-ray photoelectron spectroscopy (XPS). The electrical properties of the Cu alloy films prepared on the dielectric substrates were also evaluated. We also compared the thermal stabilities of the Cu-V/low-k/Si and Cu-V/Ta/low-k/Si samples by conducting leakage current measurements of the metal-insulator-semiconductor (MIS) structures.

2. Experimental methods

Low-k layers were grown on Si wafers using plasma chemical vapor deposition. The introduction of porosity is required to obtain films with a k value below 2.5. Pores were generated using a UV curing process. To remove the porogen, irradiation treatment was performed at 1.3×10^{-4} Pa in a vacuum chamber, which was evacuated using a rotary pump and a turbomolecular pump.

A Cu alloy with a thickness of 40 nm was then fabricated on the plasma-pretreated low-k substrates by means of magnetron sputtering using Cu (99.99%) and V (99.99%) targets. The chamber was pumped to a base pressure of 1.3×10^{-4} Pa and the working pressure was controlled at 6.6×10^{-1} Pa during the sputtering. The Cu target power was 60 W and the alloy target power was 20 W. Deposition was performed at 150 °C for 5 min. The composition of V in the Cu alloy film was 3.9 at.%. The sub-Ta layer was deposited on the low-k dielectrics using RF magnetron sputtering for 2 min. Ta films with a thickness of ~2 nm were selected for further evaluation.

After deposition of the films, the samples were annealed for 1 h where the annealing temperature was between 300 and 500 °C under vacuum. The thicknesses and the cross-sectional images of the films were examined using TEM (JEOL JEM-2100F, operating voltage = 200 kV). Energy dispersive spectroscopy (EDS) analyses were performed as part of the scanning transmission electron microscopy (STEM) investigation to obtain elemental composition maps across the interfaces. The chemical composition of each layer was investigated using AES and depth profiling analyses. For the Cu alloy samples, sputtering rates of ~5 nm/min were used for the depth profile analysis. The sheet resistance was measured using a four-point probe (JANDEL). For characterization of the chemical states of the self-formed layer, XPS (Thermo Fisher Scientific Co., theta probe base system) was performed using Al Kα radiation (1486.6 eV). To expose the self-formed layer, we utilized a simultaneous Ar etching process. The leakage current measurements of the Cu alloy/low-k/Si (MIS) structures were measured by monitoring the current-voltage (I-V) curves using an HP 4145 picoammeter/DC voltage source before and after the thermal stress process.

3. Results and discussion

The sheet resistance changes of the Cu-V/low-k and Cu-V/Ta/low-k samples were evaluated under the barrier formation conditions. Fig. 1 shows the percentage variation of the sheet resistance of the samples according to the barrier formation temperature. The change of the sheet resistance between the annealed and as-deposited samples divided by the sheet resistance of the as-deposited samples is referred to as the variation percentage of sheet resistance ($\Delta R_s/R_s\%$) and is expressed as follows [22,23].

$$\frac{\Delta R_s}{R_s} = \frac{R_{s,after\ anneal} - R_{s,as-deposited}}{R_{s,as-deposited}} \times 100\ (\%) \quad (1)$$

Cu diffuses fast in Si and forms Cu_3Si compounds at low temperatures near 200 °C, resulting in a drastic increase of the sheet resistance of the Cu film. However, the sheet resistance of the Cu-V/low-k and Cu-V/Ta/low-k samples did not increase after annealing at temperatures up to 500 °C for 1 h, indicating that there was no change in the material, either chemically or physically, such as bonding to other materials or material loss. The sheet resistance of the Cu-V alloy decreased with increasing annealing temperature. The decrease can mainly be attributed to the diffusion of a solute element to the film surface or interface between the Cu-V alloy and low-k layer. It has been reported that defect annihilation and grain growth only had relatively minor effects on the reduction of resistivity [24]. The Cu-V alloy on low-k samples was used to investigate the barrier properties in our previous study [20]. Our group reported that the amount of segregation of the V atoms at the film surface and the Cu-V alloy/dielectric interface influences the V concentration in the Cu-V alloy. This caused a different trend of the electrical resistivity of the alloy films because of the decrease of impurity scattering.

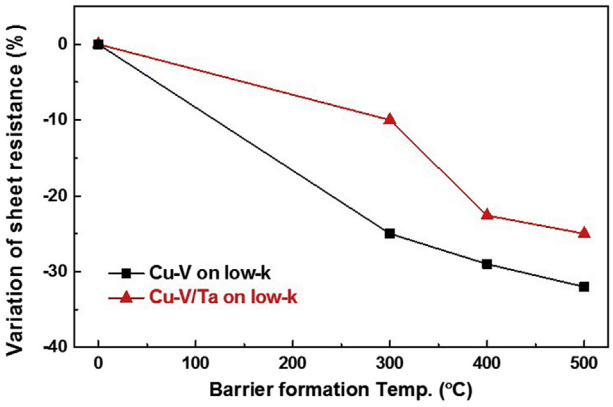

Fig. 1. Variation of the sheet resistance of the Cu-V alloy films with or without the sub-Ta layer at various annealing temperatures.