Materials Letters 196 (2017) 280–283

Contents lists available at ScienceDirect

Materials Letters

journal homepage: www.elsevier.com/locate/mlblue

Formation of silicon carbide nanowire on insulator through direct wet oxidation

Hoang-Phuong Phan [a,*], Ginnosuke Ina [b], Toan Dinh [a], Takahiro Kozeki [b], Tuan-Khoa Nguyen [a], Takahiro Namazu [c], Afzaal Qamar [a], Dzung Viet Dao [a], Nam-Trung Nguyen [a]

[a] Queensland Micro- and Nanotechnology Centre, Griffith University, Queensland, Australia
[b] Department of Mechanical Engineering, University of Hyogo, Hyogo, Japan
[c] Department of Mechanical Engineering, Aichi Institute of Technology, Toyota, Japan

ARTICLE INFO

Article history:
Received 6 February 2017
Accepted 21 March 2017
Available online 23 March 2017

Keywords:
Silicon carbide
SiC on insulator
SiC nanowires
Nanowires waveguides
LOCOS
MEMS

ABSTRACT

Silicon carbide on insulator is a promising platform for electronic devices at high temperature as well as for opto-electrical applications. Utilizing the chemical inertness of SiC, this work presents a novel technique to form cubic-silicon carbide (3C-SiC) on silicon dioxide (SiO_2) by using silicon wet-thermal-oxidation. Experimental data confirmed that SiO_2 was successfully formed underneath of 300 nm width SiC nanowires, while the properties of SiC was almost unaffected during the oxidation process. This simple technique will open the pathway to the development of SiCOI (SiC on insulator) based electrical and optical applications.

1. Introduction

Wide band gap materials such as diamond like carbon, III–nitride, and silicon carbide have been widely applied in numerous electronic devices, where hostile conditions including high power, high temperature exist [1,2]. These materials have also been employed in MEMS applications which aim at high frequency and high temperature sensing transducers. Among numerous materials, silicon carbide is a preferable choice owing to its excellent physical properties along with the availability of wafers [3,4]. Nevertheless, the main obstacles which hinder the wide applications of SiC are the high cost of wafer and low etching rate of SiC in comparison to Si.

To solve these bottlenecks, cubic silicon carbide thin films, which can be grown on a silicon substrate have been deployed as an excellent platform for MEMS [5–8]. Epitaxial SiC films grown on large scale Si wafers not only take advantage of low cost Si wafers, but also simplify the fabrication process of SiC MEMS. To make SiC devices feasible for applications in harsh environments, electrical insulators such as SiO_2 are desired to prevent the leakage current from the functional layer (SiC) to the substrate (Si). In addition, the SiC on SiO_2 platform is also of significant interest for optical applications such as SiC waveguides or photonic crystals since SiC offers a higher refractive index than SiO_2 [9–11]. To date, the most common method to form SiC on insulator is based on wafer bonding. However, wafer bonding typically requires smooth-surface treatment and additional time-consuming steps for the removal of Si. [12–15].

This letter presents a novel technique to form SiC on insulator by thermally oxidizing the Si substrate. The key concept of this technique is based on the chemical inertness of SiC which allows the material remain unchanged during the thermal oxidation process. In fact, the proposed technique is inspired by the LOCOS (local oxidation of silicon) method that has been widely employed in many CMOS (complementary metal–oxide–semiconductor) devices [16]; however, there has been no report on utilizing LOCOS into SiC material to form SiCOI. Our experimental measurements shows that thermal oxidation of silicon makes the development of SiC nano structures (e.g. nanowires) on insulator possible without the requirements of wafer-bonding and/or silicon removal. The proposed method could pave the way to the development of SiC based MEMS devices including high temperature sensors, and nanowire waveguides.

2. Methodology and fabrication process of SiNWs

Fig. 1 illustrates the methodology and fabrication process to form 3C-SiC on insulator. The idea of creating SiC on SiO_2 was motivated by the low oxidation rate of SiC with respect to Si

* Corresponding author.
E-mail address: hoangphuong.phan@griffithuni.edu.au (H.-P. Phan).

http://dx.doi.org/10.1016/j.matlet.2017.03.118
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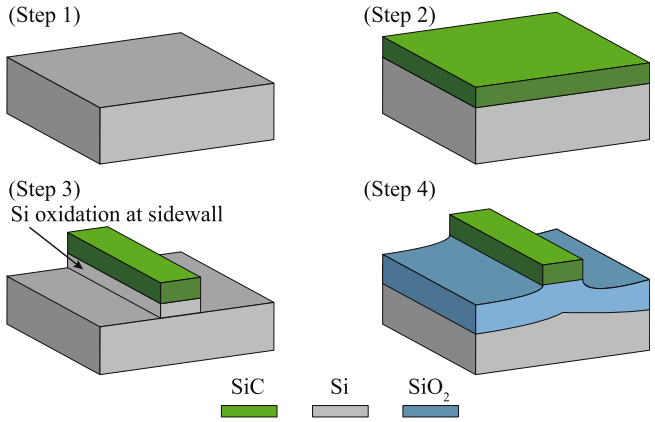

Fig. 1. The fabrication process of SiC NWs on insulator.

[17]. Furthermore, when patterning SiC, the Si substrate was also intentionally etched, forming a Si sidewall underneath SiC. This sidewall allows the thermal oxidation to occur in the lateral direction, transforming the Si layer under SiC into SiO_2. It should also be pointed out that, to make SiC fully isolated from the Si substrate, SiC structures with a narrow width are preferable as their oxidizing time is significantly reduced. Consequently, SiC nano structures such as nanowires are more well suited for the proposed technique than micro structures.

The fabrication process of the SiC on SiO_2 started from a 150 mm Si wafer treated with a standard RCA (Radio Corporation of America) process (step 1). A 3C-SiC thin film was then epitaxially grown on the Si wafer using low pressure chemical vapor deposition at 1000 °C (step 2). The detailed growth process of the 3C-SiC can be found elsewhere [18]. The thickness of the SiC layer, measured by ™NANOMETRICS Nanospec/AFT 210, was found to be 288 nm. The carrier concentration of the film was 5×10^{18} cm^{-3} measured by a hot probe technique. Subsequently, SiC nanowires were formed using FIB (focused ion beam) ™SII NanoTechnology SMI3050SE (step 3) [19,20]. After the FIB cutting process, thermal annealing at 500 °C was performed to eliminate the implanted Ga^+ ions from the Si. Finally, the patterned SiC on Si samples were wet-oxidized to form SiC on SiO_2. It should be noted that increasing the temperature could significantly reduce the oxidation time; however, the temperature needs to be limited below that used in the LPCVD process in order to prevent unexpected changes in the properties of the SiC film. Therefore, we carried out the oxidation process at 950 °C, which is below the growth temperature of 3C-SiC (1000 °C). The oxidation time for Si was estimated as follows.

Let t_{ox} be the thickness of the grown SiO_2, the thickness of the consumed Si layer is $t_{Si} = 0.44 \times t_{ox}$. Furthermore, as the oxidation occurs on both sides of the Si sidewall, the actually consumed Si layer must be larger than half of the width of the SiC nanowires. Therefore, the amount of time required to sufficiently oxidize the SiC/Si samples is:

$$t = \frac{w/2}{0.44 \times \mu_T} \quad (1)$$

where w and μ_T are the width of the SiC nanowires, and the oxidation rate of Si at degree T, respectively.

2.1. Results

Fig. 2 shows the SEM images of SiC nanowire arrays fabricated using FIB. The dimensions of each nanowire were 288 nm in thickness, 300 nm in width and 10 μm in length. The distance from the top surface of the SiC film to that of the Si substrate was also measured to be 455 nm, using ™Dektak 150. This implies that a Si sidewall with a height of 177 nm was formed underneath SiC, allowing the subsequent horizontal oxidation.

After the oxidation of Si at 950° for 60 min, the thickness of the deposited SiO_2 layer and the consumed Si layer was obtained through the following experiments. Fig. 3(a) plots the thickness of SiC before and after the oxidation, and the thickness of the as-deposited SiO_2 layer measured using the ™NANOMETRICS Nanospec/AFT 210. The similarity between the thicknesses of SiC before (288 nm) and after thermal wet-oxidation (284 nm) indicates the excellent chemical inertness of 3C-SiC with an oxidation rate of below 1 Å/min at 950 °C. On the other hand, the thickness of the as-oxidized layer was found to be 427 nm, indicating a significant oxidation selectivity between SiC and Si of approximately 1:100.

The distance between the top surface of the SiC layer and the as-oxidized SiO_2 layer was found to be 202 nm, Fig. 3(b). As a result, the thickness of the additional SiO_2 layer deposited on to the Si layer is $t_{top,ox} = 455 - 202 = 253$ nm. Consequently, the thickness of the consumed Si layer was $t_{Si} = t_{ox} - t_{top,ox} = 427 - 253 = 174$ nm. This result indicates an geometrical ratio between the SiO_2 and the consumed Si thicknesses (t_{ox}/t_{Si}) of 1:0.41, which well fits the model presented in Eq. 1 (t_{ox}/t_{Si} = 1:0.44). More importantly, the thickness of the consumed Si layer (174 nm) was larger than half of the width of SiC nanowires (150 nm), indicating that the Si layer under the SiC nanowires was sufficiently oxidized.

Fig. 3(c) presents the SEM image of the as-oxidized SiC/Si samples. It can be clearly seen from the top view of SEM that, SiO_2 was deposited on the Si substrate. A cross section of the SiC NWs was

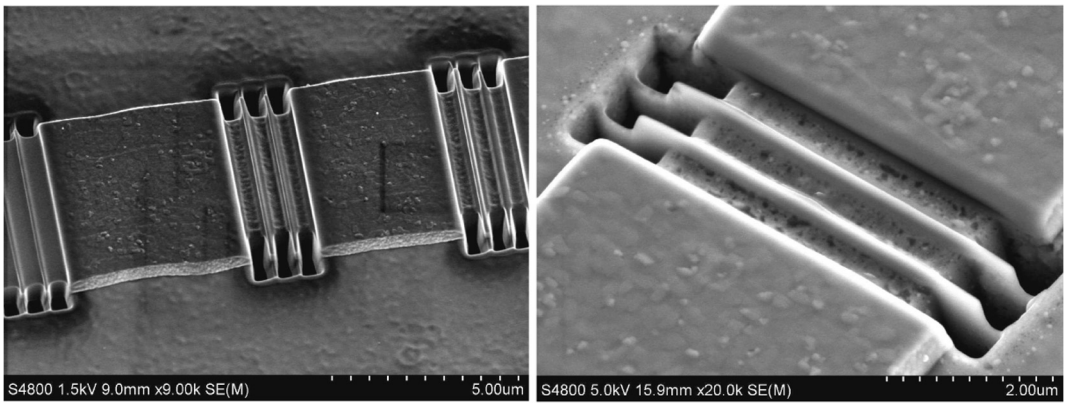

Fig. 2. SEM images of SiC nanowires prior to wet-oxidation.