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# Understanding the dependence of performance on the dielectric-semiconductor interface in pentacene-based organic field-effect transistors

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## ABSTRACT

The dependence of performance on the dielectric-semiconductor interface in pentacene-based organic field-effect transistors (OFETs) was investigated by modification of the substrate with octadecylsilane (OTS) compared with octadecyltrimethoxysilane (OTMS). The hole mobility of OFETs was enhanced from 0.43 cm<sup>2</sup>/V s to 0.72 cm<sup>2</sup>/V s when treating the substrate with OTMS versus OTS. However, the subsequent ammonia vapor did not lead to enhanced FET performance, which might be closely related to its negative influence on the pentacene growth. According to atomic force microscopy (AFM) and X-ray diffraction (XRD) measurements, flat pentacene domains with larger grain sizes and less crystal boundaries were observed for the OTS treated surface, demonstrating higher crystallinity, which may play a positive role for the charge transport and thus accounts for the improved mobility.

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## 1. Introduction

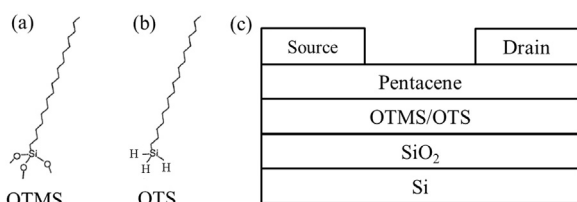
Organic field-effect transistors (OFETs) have attracted extensive attention because of their promising potential for spurring the advancement of lightweight and low-cost electronic applications, such as flat-panel displays [1–4], radio-frequency identification tags [5,6] and sensors [7–10]. As for OFETs, charge carriers are generated in a conductive channel at dielectric/organic semiconductor interface upon a proper gate bias. The modification of the interfaces, particularly the interface between the substrate and the active layer, has played an important role in enhancing the device performance since it greatly influences the carrier transport in the proximate channel. Among these, employing the SiO<sub>2</sub> surface with self-assembled layers is a common strategy to improve the interfaces in OFETs [11–16]. Alkylsilanes such as octadecyltrimethoxysilane (OTMS) and octadecylsilane (OTS) have been utilized in many studies to modify the substrate for the purpose of improving the dielectric surface characteristics [13–16], in which

the carrier trapping is reduced by passivating the hydroxyl bonds at the surface. Despite a large number of reports on the performance enhancement through surface functionalization, the origin of these effects is poorly understood, because it is a problem of “buried interface” that is commonly difficult to address.

Pentacene has served as one of the most prominent candidates for industrial manufacturing due to the high carrier mobility and commercial availability [17]. Moreover, pentacene is more susceptible to the interfacial properties than other organic semiconductors [18]. The detailed and comparative investigation about the performance variation of pentacene OFETs with the SiO<sub>2</sub> surface modified by OTMS, OTS and the subsequent ammonia vapor treatment is still lacking.

In this work, we reported that the interface between the pentacene film and the gate dielectric exerted a great impact on the performance of OFETs. Five different interfaces were studied: bare SiO<sub>2</sub>, SiO<sub>2</sub> modified with OTMS (referred to as SiO<sub>2</sub>-OTMS), SiO<sub>2</sub> coated with OTMS and subsequently exposed by ammonia vapor (SiO<sub>2</sub>-OTMS-NH<sub>3</sub>), SiO<sub>2</sub> treated with OTS (SiO<sub>2</sub>-OTS), and SiO<sub>2</sub> coated with OTS and subsequently exposed by ammonia vapor (SiO<sub>2</sub>-OTS-NH<sub>3</sub>). Pentacene OFETs based on SiO<sub>2</sub>-OTMS and SiO<sub>2</sub>-OTS exhibited the mobility of 0.43 cm<sup>2</sup>/V s and 0.72 cm<sup>2</sup>/V s, respectively, while much lower mobilities of 0.07 cm<sup>2</sup>/V s and 0.11 cm<sup>2</sup>/V s were obtained from those devices based on

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**Fig. 1.** Chemical structures of (a) OTMS, (b) OTS; (c) Device structure of pentacene-based OFETs.

$\text{SiO}_2\text{-OTMS-NH}_3$  and  $\text{SiO}_2\text{-OTS-NH}_3$ , respectively. Further study on the morphology and structure revealed that the variation in the mobility was closely related to the morphological and structural properties of the resulting pentacene films induced by the modification of the interfaces.

## 2. Experiments

### 2.1. Materials

The alkylsilane compounds, such as octadecyltrimethoxysilane (OTMS) and octadecylsilane (OTS), were purchased from J&K Chemicals and used without further purification. Pentacene was purchased from Aldrich.

### 2.2. Self-assembled layer deposition

Prior to the surface modification, the wafer was cleaned with acetone, ethanol and deionized water sequentially. OTMS and OTS were employed to modify the wafer via vapor deposition. After the modification of OTMS or OTS, the substrates were exposed to ammonia vapor for 10 h at room temperature.

### 2.3. Device fabrication

OFETs were prepared on the wafer with a 300 nm-thick thermally grown  $\text{SiO}_2$  as the gate dielectric in a bottom-gate top-contact configuration. The chemical structures of OTMS and OTS and the device architecture are shown in Fig. 1. Firstly, the substrates were subjected to different treatments. Pentacene was then thermally deposited onto the different modified substrates at a rate of  $1 \text{ \AA/s}$  under a base pressure of  $1 \times 10^{-5} \text{ Pa}$ . Finally, the source and drain electrode were obtained by evaporating gold through a shadow mask on a pentacene film with the thickness of around 40 nm. All electrical measurements were performed on Keithley 2636 source/measure units at room temperature in air. The microscopic surface morphologies were characterized by using Bruker icon Dimension with scanAsyst atomic force microscopy (AFM).

## 3. Results and discussions

As mentioned above, five different interfaces were studied in order to explore the influence of the interfacial surfaces on the device performance. Pentacene was selected as the active layer for bottom-gate top-contact OFETs. Typical pentacene devices with the channel width of  $W=2000 \mu\text{m}$  and  $L=100 \mu\text{m}$  are characterized to obtain the hole mobility in the saturation regime ( $\mu$ ), the threshold ( $V_{\text{th}}$ ), and current on/off ratios ( $I_{\text{on}}/I_{\text{off}}$ ). The output

and transfer characteristics of typical pentacene devices are shown in Fig. 2. The key parameters of the device performance are summarized in Table 1. The values reported for mobility and on/off ratio values are averages from 12 devices, and the error is the standard deviation. Pentacene OFETs based on  $\text{SiO}_2\text{-OTMS}$  and  $\text{SiO}_2\text{-OTS}$  exhibited mobility of  $0.43 \pm 0.03 \text{ cm}^2/\text{V s}$  and  $0.72 \pm 0.02 \text{ cm}^2/\text{V s}$ , respectively. In contrast, much lower mobilities of  $0.07 \pm 0.004 \text{ cm}^2/\text{V s}$  and  $0.11 \pm 0.03 \text{ cm}^2/\text{V s}$  were obtained from those devices based on  $\text{SiO}_2\text{-OTMS-NH}_3$  and  $\text{SiO}_2\text{-OTS-NH}_3$ , respectively. Among these, the mobility of the device based on  $\text{SiO}_2\text{-OTS}$  is the highest. Thus, OTS is superior to OTMS in terms of the substrate modification, largely reducing dielectric surface traps. Unexpectedly, based on the results, the exposure of ammonia is not beneficial for improving the device performance in terms of the mobility.

For the purpose to understand the origin of the difference in device performance, atomic force microscopy (AFM) was performed. Fig. 3 shows the AFM images of pentacene layers grown on five different dielectric-semiconductor interfaces. As clearly demonstrated, various morphologies were observed for pentacene films. Without any treatment of  $\text{SiO}_2$ , the pentacene molecules displayed very small domains with large voids, which was detrimental for charge carrier transport (Fig. 3a). In the case of  $\text{SiO}_2\text{-OTMS}$  interface, terrace-like domains were observed with some grain boundaries and the average domain size of the top terraces is about 280 nm (Fig. 3b). In contrast, as for  $\text{SiO}_2\text{-OTS}$  interface, the morphological feature with larger grain sizes (about 390 nm) and less crystal boundaries are discernible compared with that of  $\text{SiO}_2\text{-OTMS}$  interface (Fig. 3d). Under this circumstance, flat pentacene domains become very prominent in the surface, manifesting the most expanded domain size of each stack. It is worthwhile to mention that this thin film morphology is deemed as the optimal one for OFET's electrical performance. However, the conglomerated island-type pentacene domains with smaller sizes and more boundaries are noticed for  $\text{SiO}_2\text{-OTMS-NH}_3$  and  $\text{SiO}_2\text{-OTS-NH}_3$  interfaces, exhibiting vertical growth. Under this condition, the top terrace is much smaller than the bottom one during the vertical growth. It is indicated that the ammonia vapor treatment for OTMS- and OTS-functionalized surfaces is not beneficial for the pentacene growth. According to the results, AFM images matched well with the electrical performance of OFETs.

In order to further understand what happen in the film after modification on the dielectric, we have performed XRD characterizations on the pentacene layers grown on five different dielectric-semiconductor interfaces (Fig. S1). It is demonstrated that the semiconductor crystallinity in the OFETs studied here is strongly driven by the dielectric-semiconductor interface. The pentacene film on  $\text{SiO}_2\text{-OTS}$  exhibits one-order of magnitude higher diffraction peaks than that on  $\text{SiO}_2\text{-OTMS}$ . By contrast, lower diffraction peaks are observed for the pentacene films on  $\text{SiO}_2\text{-OTMS-NH}_3$  and  $\text{SiO}_2\text{-OTS-NH}_3$ . The XRD spectra in pentacene films grown on  $\text{SiO}_2\text{-OTS}$  exhibit a series of sharp (00k) peaks. It is implied a higher level of crystallinity, which in turn can explain the higher mobility in OFETs.

## 4. Conclusion

The influence of the dielectric-semiconductor interface on pentacene growth and the performance of pentacene-based transistors was investigated by employing OTMS, OTS and the subsequent ammonia vapor treatment on the gate dielectric. The

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