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Plasma-enhanced chemical vapor-deposited organic dielectric layer for low voltage, flexible organic thin-film transistor

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ABSTRACT

We investigated the electronic properties of pentacene-based organic thin-film transistors (OTFTs) incorporated with an organic dielectric layer (ODL) fabricated using a homemade, cold plasma–enhanced chemical vapor deposition system. Ar-carried trimethylaluminum monomer was introduced into an evaporator mixer controlled at 130 °C, and an ODL was deposited on Si- or indium tin oxide (ITO)–coated plastic substrate under N_2 plasma. High radio frequency power (100 W)-deposited ODL (dielectric constant $\kappa = 1.6$) supported the fabrication of pentacene-based OTFT on Si substrate at low voltages (<1.5 V). The decreased deposition time (10 min) reduced the film thickness of the ODL (95 nm), thereby increasing its dielectric constant to 3.3. We also deposited ODL on ITO–coated plastic substrate to fabricate a flexible OTFT with a mobility of 2.1 cm^2/Vs and an on/off current ratio (I_{on}/I_{off}) of 10^3.

1. Introduction

Organic thin-film transistors (OTFTs) have been intensively studied [1–3] and are essential components for next-generation electronic devices because of their superior properties of low-cost fabrication, light weight, and flexibility. However, the high operational voltage (>5 V) caused by the low charge carrier mobility of organic semiconductors limits the practical use of OTFTs in portable electronic devices. Several studies [4–14] have demonstrated that increasing the charge carrier mobility and decreasing the dielectric layer thickness can efficiently lower the operational and threshold voltages (V_{th}). Optimizing the surface morphology of the organic semiconducting layer and reducing the density of the charge traps at the dielectric–semiconductor interface can also reduce the operational and threshold voltages. Organic dielectric layer (ODL) used in OTFT have shown better performances [15–19]; however, inhomogeneous ODL was obtained by the sol-gel or spin-coated process [20,21]. The technique of plasma-enhanced chemical vapor deposition (PECVD) has shown the ability of improving the boundary between ODL and charge conducting layer and fabricating the electron conducting layer [22,23]. In this study, we used an ODL fabricated through plasma-enhanced chemical vapor deposition (PECVD) in pentacene-based OTFTs and exhibited a low threshold (<0.4 V) and operational voltage (<1.5 V) as a gating dielectric. We also fabricated a flexible pentacene-based OTFT on plastic substrate using ODL as a gating dielectric; the fabricated films had an enhanced carrier mobility of 2.1 cm^2/Vs. The improved electronic properties of the fabricated OTFTs are due to the generation of a trap-free interface between the ODL and pentacene.

2. Experimental

p-Type doped (0.001–0.005 Ω cm) (100) Si wafer and indium tin oxide (ITO) (8 Ω cm)-coated polyethylene terephthalate (PET) were used as device substrates. The gating dielectrics were fabricated using a homemade, cold PECVD system with Ar-carried trimethylaluminum (TMA) monomer under N_2 plasma at a gas flow of 10 mln/min, liquid flow of 5 g/h, and purge pressure of 4 kg/cm^2; these conditions were fixed and controlled using a mass flow meter/controller equipped with an evaporator mixer maintained at 130 °C (M12-RAD-22-0-S, F-201CV-200-RAD-22-V, W-102A-222-K, Bronkhorst, Taiwan). The surface morphologies and thicknesses of ODL were controlled by varying the deposition power and time. The composition of ODL was C (82%):N (10%)/O (8%) examined by XPS method. After the ODL was grown on Si or ITO-PET substrate, pentacene was deposited on the ODL through thermal evaporation. Gold electrodes of 40 nm thickness were thermally evaporated on pentacene through a shadow mask of drain–source contact with channel length (L) and width (W) of 100 and 1000 μm, respectively. Fig. 1 shows a schematic and images of the bottom-gated OTFT devices with Si and ITO-coated PET substrates.

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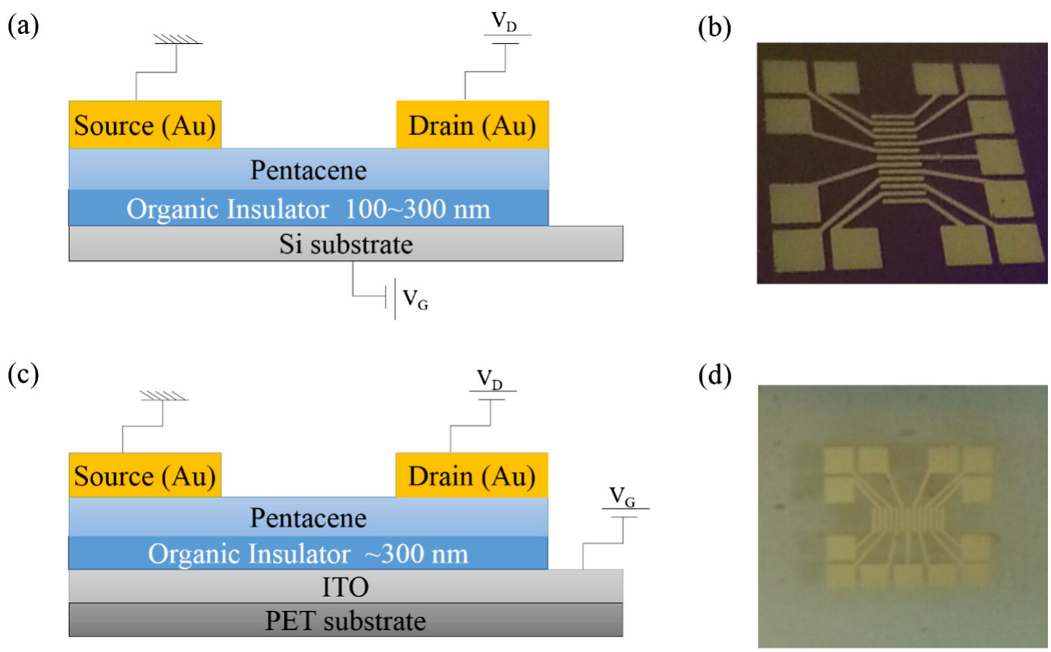

Fig. 1. (a) and (c) Device structures and (b) and (d) images of OFTF with Si and ITO-coated PET as substrates.

3. Results and discussion

Fig. 2 shows the drain–source current (I_D) and drain–source voltage (V_D) characteristics of OTFT on Si substrate with PECVD-ODLs as a function of the gating voltage (V_D) in which the ODL was fabricated by changing the radio-frequency (r.f.) power during PECVD process. Low r.f. power (25 W)-deposited ODL in OTFT did not exhibit current saturation when V_D was varied from 0 to −1 V (Fig. 2(a)). However, high r.f. power (100 W)-deposited ODL in OTFT exhibited typical p-type pentacene-based OTFT when working in accumulation mode under a low gating voltage (V_G) of −1 V (Fig. 2(d)).

Typically, a thinner layer of gating dielectric results in higher capacitance values and enhances the electronic performance of OTFT. Fig. 3(a) shows the output characteristics of an OTFT on Si substrate with a 95-nm PECVD-ODL with a dielectric constant of 3.3, which is larger than the dielectric constant (1.6) of a 300-nm PECVD-ODL. Fig. 3(b) illustrates the transfer characteristics of the 95-nm PECVD-ODL OFTF as a gating dielectric, which exhibits a low V_{th} of −0.48 V and on/off current

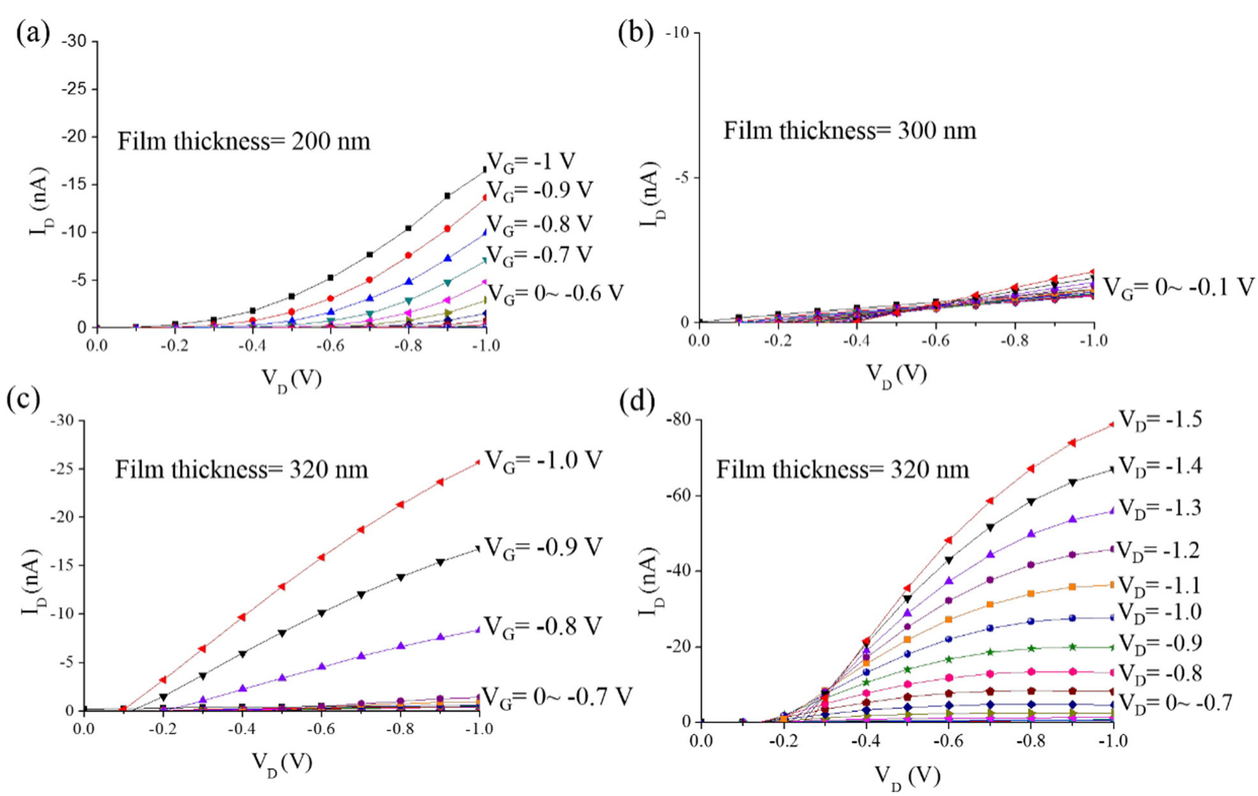

Fig. 2. Current–voltage characteristics of OTFT on silicon substrate with PECVD-ODL deposited at r.f. powers of (a) 25 W, (b) 50 W, (c) 75 W, and (d) 100 W.

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