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Accurate modeling of gate tunneling currents in Metal-Insulator-Semiconductor capacitors based on ultra-thin atomic-layer deposited Al_2O_3 and post-metallization annealing

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Even though the introduction of high-dielectric constant (high-κ) materials has enabled the continuous advancement of Moore's Law into the nanometer regime, accurate predictions ensuring long-term operation of these devices is now more complicated due to several physical and electronic considerations: 1) precise atomic control of the high-k material in the ultra-thin regime (thickness, stoichiometry, dielectric constant, etc), 2) excessively large gate leakage currents, 3) appearance of several conduction mechanisms able to degrade the performance and reliability of the devices, 4) interfacial defects at the high-k/silicon interface and 5) low thermodynamic stability of the high-k materials after exposure to inherent thermal treatments during several processing stages. In order to provide better device performance/reliability predictions, this work offers a consistent and accurate verification of the precise carrier conduction mechanisms of Metal-Insulator-Semiconductor (MIS) capacitors (biased under substrate injection conditions) when ultra-

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