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Mapping and comparison of the shortcomings of kesterite absorber layers, and how they could affect industrial scalability

Remi Aninat *, Luis-Enrique Quesada-Rubio, Emilio Sanchez-Cortezon, Jose-Maria Delgado-Sanchez

Abengoa, C/Energía Solar 1, 41013 Sevilla, Spain

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ABSTRACT

Kesterite absorber layers for thin film solar cells are promising in terms of cost and material abundance, but still lag relatively far behind $Cu(In,Ga)(S,Se)_2$ in terms of device efficiency. This raises questions about their potential for large-scale production. This work aims at assessing the challenges of scaling up the existing Physical Vapor Deposition processes of $Cu_2ZnSnSe_4$, Cu_2ZnSnS_4 or $Cu_2ZnSn(S,Se)_4$ for industrial fabrication. The main issues that can affect kesterite and their causes are listed and prioritized in terms of criticality for the performance, using the methodology of Design Failure Mode and Effects Analysis. This analysis indicates, in particular, that bandgap and potential fluctuations are, to date, the most critical risk factors for the absorber, because of the inability to prevent them in the current state of our understanding. Applying the acquired knowledge to the known fabrication routes for kesterite, we analyze how some of these shortcomings can originate from unsuitable metallic ratios in the precursor and the absorber due in particular to the Sn loss in kesterite fabrication processes. In the most efficient devices to date, this loss forces the sequential route (i.e. deposition/selenization) on what are historically 1-stage processes (co-evaporation, reactive sputtering) developed for industrial $Cu(In,Ga)(S,Se)_2$ fabrication.

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1. Introduction

$Cu(In,Ga)(S, Se)_2$-based (CIGS) photovoltaic devices have now achieved lab-scale efficiencies higher than any other thin film device with a current 22.6% efficiency record [1,2], thanks to the implementation of new steps into the fabrication process, such as the KF treatment most recently [3,4], which could soon benefit the industry. However, CIGS contains a large proportion of indium, which is already extensively used in the LCD industry, and scarce in the earth's crust [5]. The price of this element could therefore increase drastically in the future and impact the price or the production capacity of CIGS. Assuming that efficiencies comparable to CIGS can be achieved, its close cousin $Cu_2ZnSn(S,Se)_4$ (CZTS) would be a valid, more earth abundant alternative to CIGS. To date, the best efficiencies achieved in the lab by CZTS-based devices (12.7% record for a $Cu_2ZnSn(S,Se)_4$ device [6]) are modest in comparison to CIGS. This is still insufficient to scale up the process, especially considering the efficiency gap between lab-scale device and industrially produced modules observed for CIGS. However, it is important to evaluate the scalability of the processes being used at this early stage, in order to start tackling some of the challenges that future attempts to scale-up could be faced with. This work presents a Design Failure Mode and Effects Analysis (D-FMEA), as a step towards more specific and technical scale-up analyses (e.g. process FMEA).

2. Methodology

This paper focuses on the kesterite absorber layer, including its interfaces with the buffer layer and the back contact to account for the large interplay between these interfaces, the bulk and the device properties. The methodology of D-FMEA is used to list out and prioritize the different issues that have been reported for this material [7]. It is a semi-quantitative method, in the sense that figures of merit (FOM) used to prioritize the failure are assigned values in a systematic way, but using mainly qualitative considerations. The aim is to prioritize the order in which the failures must be addressed and to eliminate the most important ones in priority.

A set of three figures of merit (FOM) was used for the D-FMEA study:

- Severity (S), how strongly the failure affects the performance of the device
- Probability of occurrence (O), how likely is the failure to occur
- Non-detectability (D), how difficult it is to detect and overcome the failure.

* Corresponding author.
E-mail address: remi.aninat@abengoa.com (R. Aninat).

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A more synthetic FOM, called risk priority number, $RPN = S \times O \times D$, is also used to magnify the differences between failures. The tables used to assign the FOM were made specific for this work, in order to assign FOMs more unambiguously (Table 1). A practical efficiency goal was needed to assess the Severity of the different failure modes of CZTS based on the literature bearing in mind that the record CZTS devices are still largely flawed by failure modes. We chose the record CIGS efficiency (22.6% [2]) as the "reference", that is, the efficiency at which the CZTS would be considered to have no failure. This is a simplification, since the current champion CIGS is still far from the Shockley-Queisser limit, and is therefore still flawed. However, at this early stage of maturity, the use of CIGS as a reference is very useful in providing realistic targets for V_{OC} and other electrical properties. The Occurrence corresponds to how often the failure is reported in state-of the art devices or, in the case of secondary phases (SP), to how close the compositions leading to these SP are to the composition generally targeted in the literature (Cu/(Zn + Sn) = 0.8, Zn/Sn = 1.2). The non-Detectability depends on either the difficulty to detect the failure or the difficulty to overcome it once detected (whichever gives the highest figure). Note that the D-FMEA presented is based on the data available at the time of the redaction and could evolve as new information arises.

3. Results

3.1. Shortcomings of CZTS-based devices

The main issues ("failure modes") of kesterite absorber layers have been widely investigated in the past few years. The most important one is a too large open-circuit voltage (V_{OC}) deficit [8–11] (Fig. 1). Other shortcomings, only present in few of the best devices to date, are a too high series resistance (R_S) [12–14] and a too low short circuit current density (J_{SC}) [14,15].

The failure modes and their causes are mapped out in Fig. 2. The V_{OC} can be affected by bulk recombination mechanisms, either within the grains [10,17–27] or at the grain boundaries [28–31], or by front interface recombinations [10,20,32–35]. A high R_s can be due to a potential barrier at the back contact [12,36] or at the heterojunction [37,38], while low J_{SC} can be due to a too thin absorber, although some reports suggest that the material performs well even for relatively thin absorbers [15,39,40]. Low J_{SC} and V_{OC} are mitigated in the best CIGS devices by using the "notch" profile, with a back surface field (BSF) (achieved with a Ga/In gradient at the back) and a bandgap rise at the heterojunction (achieved with a S/Se increase) [41]. In CZTS, calculations indicate that the conduction band offset required to generate the BSF is better achieved by replacing some of the Sn with other group IV elements [42,43]. In practice however, it has only been successfully demonstrated on low efficiency devices, to our knowledge [44]. Furthermore, VOC improvements were reported in CZTS alloyed uniformly throughout the absorber's depth with Ge [45].

Table 1
Scales used to assign the figures of merit "severity", based on the power conversion efficiency (PCE), "occurrence" and "non-detectability".

Severity		Occurrence		Non-Detectability	
PCE<20% of reference	10	Almost 100% chance to occur.	10	Cannot be detected - Cannot be controlled	10
PCE<20% of reference	9		9	Detected indirectly - If detected, solution unknown	9
20%<PCE<50% of reference	8	High. Happens repeatedly. Imperfect design.	8	Detected directly with one or a combination of exotic techniques - Requires extensive study to overcome	8
	7		7		7
	6	Moderate. Advanced design. 5 is given by default if occurrence unknown	6	Detected with a combination of standard techniques - Requires non - trivial changes	6
50%<PCE<80% of reference	5		5		5
	4		4	Detected with standard techniques - Corrected with trivial design adjustments	4
80%<PCE<90% of reference	3	Low. Proven design	3		3
	2		2		2
90%<PCE<100% of reference	1	Remote. Very unlikely	1	Totally under control	1

3.2. Design failure mode and effect analysis

From the failure mapping of Fig. 2, the D-FMEA methodology was then used to prioritize the different failure modes. The results for the failure modes most relevant to this work and sufficiently supported by data are summarized in Table 2 and Fig. 3.

Band tailing, due to either electrostatic potential fluctuations [17,63] (EPF) or bandgap fluctuations [16,21] (EgF), is the most critical failure mode because it cannot yet be avoided. The question of its severity is open. Repins et al. reported low carrier lifetime in co-evaporated samples, which could originate from EgF, and calculated that solving this issue would only lead to efficiencies in the 11–13% range [46], while Gokmen et al. report low mobility issues in hydrazine-processed samples, which they attribute to EPF, and calculated that it could account almost fully for the V_{OC} deficit in the lower bandgap kesterite but not at the higher S/Se ratios [17]. The presence of deep defect(s), corroborated by several labs [16,25,45], would also be very detrimental (higher S), especially near the heterojunction [47]. Although grain boundaries in CZTS were reported to have favorable electrical properties [30,31], several labs observed efficiency improvements with increasing grain size [28,29].

3.3. Consequences on scale-up

Studying the correlations between process parameters and device properties, which would be required to study comprehensively the risks for scale up, is beyond the scope of the D-FMEA. Furthermore, how the future paths for efficiency improvement will affect the process and its scalability is unknown. However, some preliminary conclusions can be drawn from the analysis presented here. A large part of the failure modes of Fig. 3, e.g. secondary phases, grain boundary recombinations or lattice disorder (causing EgF) can be affected by the metal ratios in the precursor or the absorber [23,64]. Furthermore, the region of compositions yielding good efficiencies is significantly narrower than in CIGS [65]. Therefore, the volatility of Sn (as SnSe) at the temperatures required to form good crystallinity CZTS [66] has resulted so far in the best devices being produced by 2-step, not only for the selenization of stacked layers [67] but also for traditionally 1-step processes like co-evaporation [68] or reactive sputtering [58]. Sn losses are therefore a challenge for the scale up of the kesterite fabrication in general, demanding higher control over the deposition and selenization conditions than in CIGS processes, but could affect co-evaporation and reactive sputtering more strongly if low-cost engineering solutions cannot be found to make them as efficient by 1-step. Indeed, companies such as Manz or Miasolé already use 1-step co-evaporation and reactive sputtering (respectively) for fabricating high efficiency CIGS modules [69], and adding an extra annealing step for growing more crystalline CZTS could impact the throughput and the price. Deep defects, on the other hand, would be a good candidate to account for the large V_{OC} deficit in CZTS, since they can have a large impact on the V_{OC}, especially if near the surface (e.g. Shockley-Read-Hall). However they are still largely under investigated, so that the question of their nature, occurrence and severity are not fully resolved. All these issues would have

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