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High performance a-InZnSnO thin-film transistor with a self-diffusion-barrier formable copper contact

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ABSTRACT

A low resistivity copper (Cu) film was used as a source/drain contact layer to fabricate high performance amorphous In-Zn-Sn-O (a-IZTO) thin-film transistors (TFTs). The calcium (Ca)-doped Cu films greatly simplified the conventional Cu/diffusion barrier stack structure and process, which allowed the production of promising a-IZTO TFTs with a saturation mobility of 22.8 cm^2/Vs and an $I_{ON/OFF}$ ratio of 10^8. Furthermore, the a-IZTO TFTs with the Ca-doped Cu contact exhibited better gate bias thermal stress-induced stabilities than those with the pure Cu contact. This was attributed to the effective formation of a self-diffusion CuO_x barrier at the Cu/IZTO interfaces.

1. Introduction

Since Hosono et al. discovered a three-component oxide semiconducting material called amorphous In-Ga-Zn-O (a-IGZO) [1] with high electron mobility (~10 cm^2/Vs) in 2004, there has been increasing interest in a-IGZO semiconductors as an emerging channel material that can replace a-Si. Owing to its favorable material properties, such as high electron mobility and high transmittance, as well as the fact that it allows low-temperature, large-area deposition through sputtering, oxide semiconductors are not only suitable for the production of large-sized liquid crystal display (LCD) panels, but are also used as an essential channel material for organic light-emitting diodes (OLEDs), transparent displays and flexible displays [2–3]. An a-IGZO semiconductor (In: Ga: Zn = 1:1:1) currently used in mass production has a 20 fold higher mobility than that (~0.4 cm^2/Vs) of a-Si based thin-film transistors (TFTs). Its mobility, however, is still inferior to low-temperature polycrystalline Si (LTPS), which has prevented its use as a replacement for LTPS. For this reason, amorphous In-Zn-Sn-O (a-IZTO) has been studied extensively as a promising channel layer for high-end applications because it exhibits high mobility (>40 cm^2/Vs) without sacrificing the $I_{ON/OFF}$ modulation ratio (>10^8) [4].

Cu interconnection metallization also plays an important role toward large-area, ultra-high definition and high-frame rate active-matrix LCD and OLEDs, because of their low resistivity (~1.7 μΩ·cm), high corrosion resistance, and low material cost. The critical problems, such as high diffusivity in semiconductor (Si or IGZO) and poor adhesion to bare glass and SiO_2 insulators, however, prevent the direct use of single layer Cu films as a source/drain (S/D) electrode on the semiconductor. Instead, rather complicated stack structures involving the diffusion barrier and adhesion layer, such as titanium (Ti) [5], molybdenum (Mo) [6], tantalum (Ta) [7], and molybdenum titanium (MoTi) [8] have been used. Currently, the stack structure of Cu/Ti or Cu/MoTi is used in the production of Si and IGZO TFTs. Despite this, stack-structure-related issues, including high manufacturing cost, low process margin during etching, and reduced productivity still need to be resolved. An approach of copper alloy-based materials to overcome these limitations is important in the field of metal oxide TFTs. The use of Ca-doped Cu films as the S/D electrode in the conventional IGZO semiconductors was previously reported [9]. The field-effect mobility of an IGZO TFTs was shown to be enhanced from 5.3 cm^2/Vs (conventional Cu S/D electrode) to 16.0 cm^2/Vs by adopting the Ca-doped Cu S/D electrode [9]. Because a-IZTO system can offer a substantially higher field-effect mobility than a-IGZO with a comparable In fraction, the feasibility of Ca-doped S/D electrode into the a-IZTO TFTs system needs to be investigated.

This study examined the suitability of Ca-doped Cu metallization into the a-IZTO semiconductor as a high mobility channel material. The effects of the annealing temperature on the interfacial properties between Ca-doped Cu and a-IZTO were examined. The high field-

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effect mobility of 22.8 cm^2/Vs was achieved for the a-IZTO TFTs with Ca-doped Cu S/D contact by optimizing the annealing temperature. In addition, the IZTO TFTs with the Ca-doped Cu S/D electrode exhibited better stability against an external positive and negative gate bias stress duration compared to that of the control a-IZTO device with the conventional Cu S/D electrode.

2. Experimental

The thermal chemical vapor deposited SiO_2 film (100 nm) on the Si substrate was used as the gate dielectric, where the heavily doped p-type Si itself acts as a gate electrode. Prior to channel formation, the SiO_2/Si substrate was cleaned ultrasonically in acetone and methanol, and then rinsed with de-ionized water for 10 min. An a-IZTO film was prepared by rf magnetron sputtering at room temperature. A 3 inch diameter IZTO ceramic target (In: Zn: Sn = 20:40:40 at.%) was used. The chamber pressure and rf power were 0.40 Pa and 100 W, respectively. The fabricated a-IZTO thin films were pre-annealed in a vacuum ambient at 350 °C for 15 min. For the S/D electrodes, 200-nm-thick Cu and Cu-Ca alloys were deposited by dc magnetron sputtering. Both the channel and S/D regions were patterned using shadow masks. The TFTs were annealed in a vacuum ambient at 100 and 250 °C for 10 min.

Transmission electron microscopy (TEM) analyses for the Cu/IZTO/Si stacks were carried out on a FEI Tecnai F30 microscope operating at 200 kV. The TEM samples were prepared using conventional in-situ FIB method. The depth profiles of the Cu/IZTO/Si stacks were analyzed by energy dispersive X-ray spectroscopy (EDX), which is attached to FEI Tecnai F30 and secondary ion mass spectroscopy (SIMS, CAMECA, IMS 7f). Operation voltage, current and raster size of primary Cs^+ source during SIMS analysis were 4 kV, 10 nA and 200 μm × 200 μm, respectively. The transfer and output characteristics were measured using a semiconductor parameter analyzer (Agilent 4145HP).

3. Results and discussion

The adhesion strengths of the Cu films on the SiO_2/Si substrate were evaluated. Fig. 1 shows the cross-cut adhesion test results for the Cu and Ca-doped Cu films using 3 M tape. In the case of the Cu film on the SiO_2/Si substrate, small portion of the deposited film has flaked along the edges. In contrast, the Ca-doped film on the SiO_2/Si substrate exhibited the good adhesion property where the edges of the cuts are smooth and none of the squares of the lattice is detached. This result clearly indicated that the Ca-doped Cu film had the better mechanical adhesion property than the Cu film presumably due to the chemical diffusion and/or interaction of Ca atom with the substrate in the Cu film.

Fig. 2 shows the representative transfer and output characteristics of the a-IZTO TFTs with the different S/D electrode materials. The a-IZTO TFTs with an ITO S/D electrode exhibited the best electrical performance: the μ_{FE}, *SS*, V_{TH} and $I_{ON/OFF}$ ratio were 30.1 cm^2/Vs, 0.22 V/decade, 0.5 V and 5×10^8, respectively, as shown in Fig. 2(a) and Table 1. The high mobility of 30.1 cm^2/Vs can be attributed to the low effective electron mass in an indium-based oxide and the efficient intercalation of the *5s* orbital of In^{3+} and Sn^{4+} ions [10]. On the other hand, the device performance of the control IZTO TFTs with the pure Cu S/D electrode annealed at 250 °C was deteriorated: the μ_{FE} and *SS* values were 18.2 cm^2/Vs and 0.56 V/decade (see Fig. 1(b) and Table 1). Moreover, the V_{TH} value was positively displaced to 2.9 V. Obviously, the direct contact between the a-IZTO and Cu film deteriorated the device performance of the resulting TFTs, which can be attributed to the thermal migration of Cu atom into the underlying a-IZTO contact region and/or toward the lateral a-IZTO channel layer. The Cu atom was well-known to diffuse into the IGZO film during thermal annealing whereas the inter-diffusion and interfacial reaction was strongly prevented for the Mo/IGZO stack [8,11]. It is important to discuss the electrical role of Cu atom in the metal oxide semiconductor. The thermally or electrically incorporated Cu in the metal oxide semiconductor has been reported to act as the trap states in the forbidden bandgap [11–14]. Therefore, the reduced mobility and the stretch-out of the subthreshold drain current characteristics for the device with the Cu S/D contact is consistent with the Cu migration-induced trap creation near the IZTO channel. The fast bulk trap density (N_{SS}) in the forbidden gap of a-IZTO semiconductor and semiconductor-insulator trap density (D_{it}) can be estimated from the following equation [15].

$$SS = qk_BT(N_{SS}t_{ch} + D_{it})/[C_i \log(e)] \quad (1)$$

where q is the electron charge, k_B is Boltzmann's constant, T is the absolute temperature, and t_{ch} is the channel layer thickness. Because the N_{SS} and D_{it} cannot be determined simultaneously from the *SS* value, the maximum D_{it} ($D_{it,max}$) value in the a-IZTO TFTs was calculated by setting the N_{SS} value to zero. Likewise, the maximum $N_{SS,max}$ value was estimated by setting the D_{it} value to zero. Thus, the $N_{SS,max}$ and $D_{it,max}$ values are larger than the actual N_{SS} and D_{it} values in the a-IZTO TFTs. The $N_{SS,max}$ ($D_{it,max}$) values for the devices with the ITO, Cu and Ca-doped Cu S/D contacts were 2.7×10^{17} eV^{-1} cm^{-3} (8.0×10^{11} eV^{-1} cm^{-2}), 6.8×10^{17} eV^{-1} cm^{-3} (2.0×10^{12} eV^{-1} cm^{-2}) and 6.3×10^{17} eV^{-1} cm^{-3} (1.9×10^{12} eV^{-1} cm^{-2}), respectively. Thus, the amount of the Cu migration-created trap states ($\Delta N_{SS,max}$) would be roughly estimated to be 4.1×10^{17} eV^{-1} cm^{-3}. However, whether the Cu-related defects act as either donor-like or acceptor-like traps is still under debating [11–14]. Jeong et al. reported that the Cu incorporated into a-IGZO channel layer acts as the donor-like traps [14], which inferred from the fact that the negative V_{TH} shift of the transfer characteristics and the simultaneous increase in the drain current as the drain-to-source voltage increases. On the other hand, the entirely different acceptor-like trap behavior of the thermally diffused Cu atom was also observed for the a-IGZO [11] and zinc tin oxide semiconductor [7]. In this study, the

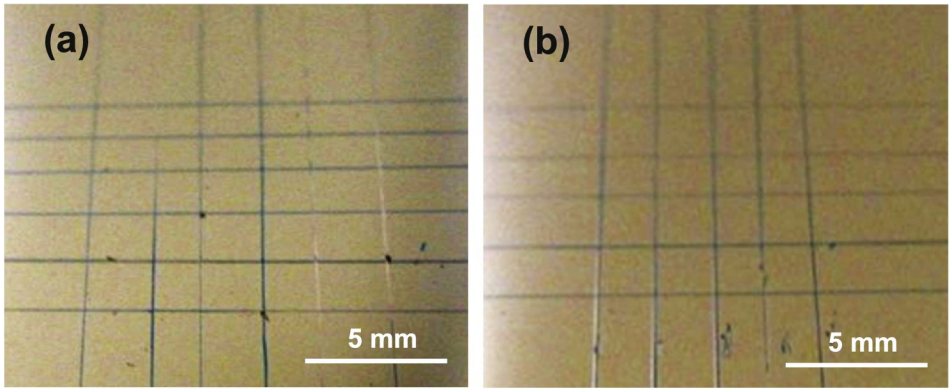

Fig. 1. Adhesion test results of (a) Cu film and (b) Ca-doped Cu film with the SiO_2/Si substrate using 3 M tape.

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