Thin Solid Films 636 (2017) 485–489

Contents lists available at ScienceDirect

Thin Solid Films

journal homepage: www.elsevier.com/locate/tsf

The effect of gate dielectric deposition at different vacuum conditions on the field-effect mobility of pentacene based organic field effect transistors

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ARTICLE INFO

Article history:
Received 29 October 2016
Received in revised form 27 June 2017
Accepted 27 June 2017
Available online 28 June 2017

Keywords:
Organic thin film transistor
Pentacene
Field-effect mobility
Surface energy
Trap limited transport
Atomic force microscopy

ABSTRACT

Pentacene based organic field effect transistors with polyvinyl phenol gate dielectric are fabricated by controlling the dielectric surface energy and grain size of the first monolayer of pentacene. In this work, we introduce a novel approach to tune the surface energy of the polymer dielectric. This is performed by baking the polymer dielectric, polyvinyl phenol, at different vacuum conditions at 160 °C before the deposition of pentacene layer. After the deposition of pentacene, these devices exhibit dramatic improvement of carrier mobility and an extraordinary change in electrical characteristics. This includes an enhancement of carrier mobility as high as 400% increase from 0.53 cm^2/Vs for low vacuum (high surface energy of the gate dielectric) to 2.02 cm^2/Vs for high vacuum (low surface energy of the gate dielectric) baking of polyvinyl dielectric thin film. It has been observed from the atomic force microscopy that the carrier mobility has a one to one correspondence with the grain size of the first monolayer. That is the carrier mobility increases with the increase in grain size. This fact is further interpreted in terms of the trap limited transport model proposed by Horowitz et.al.

1. Introduction

Pentacene based organic field effect transistors (OFETs) have attracted considerable attention in recent years. This is because of their low cost, light weight and flexibility, which finds applications in electronics and display industry [1–3]. The most outstanding issues in the field of organic semiconductor [4–6] are the field effect mobility, the on–off ratio and the threshold voltage. The appropriate tuning of these values is not only important from the application point of view, but also crucial in terms of fundamental point of view. Hence the exploration of the structure property relationship becomes tremendously significant at the semiconductor dielectric interface, where actually the charge transport occurs [7–9]. The conducting channel lies at the interface. The quality of the channel is determined by the interface roughness, grain size of the monolayer, surface energy and charges at the interface [10–18]. In this regard, the choice of polymer dielectric offers the advantage of being solution processable and applied by spin coating methods. Moreover they can be used to generate flexible devices. Amongst many polymers, the PVP (polyvinyl phenol) is mostly preferred because the spun on PVP generates smoother surface (rms ~3 nm) on rough gate electrodes (rms ~15 nm) [19]. Pentacene grown on these produces devices with high mobility. Recently we had reported the fabrication of such pentacene OFETs with PVP dielectrics and different source drain electrodes [20]. However, until now, there had been very few efforts to explore the techniques to control the gate dielectric surface energy [21] and hence to influence the grain size of pentacene monolayer, which would have a direct impact on the electrical transport of the PVP based pentacene OFETs.

In this manuscript, we report a new approach for controlling the surface energy of the gate dielectric by altering the fabrication conditions. By fabrication conditions, we refer to the baking of polyvinyl phenol dielectric under high (1.33×10^{-4} Pa) vacuum and low (1.33 Pa) vacuum conditions at a temperature of 160 °C. A difference of 4–fold increase in mobility is obtained. Moreover the magnitude of the mobility is found to be 2.02 cm^2/Vs. This is the highest value reported in the literature till date for pentacene based PVP insulated transistor with ITO as the gate electrode.

2. Fabrication methodology

Fig. 1 shows a schematic cross section of pentacene OFET. The fabrication procedure starts with a bare glass substrate coated

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http://dx.doi.org/10.1016/j.tsf.2017.06.054
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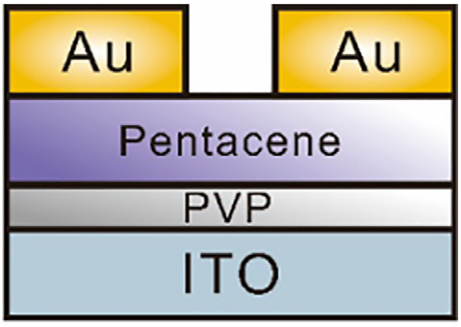

Fig. 1. Schematic cross section of a pentacene based OFET with PVP gate dielectric.

Table 1
Electrical characteristic data for pentacene based transistor with PVP gate dielectric.

	On-off ratio	V_{TH} (V)	μ (cm^2/Vs)
Low-vacuum	3100	−1.29	0.53
High-vacuum	15,028	−4.08	2.02

Table 2
Contact angles and surface energy of PVP dielectric under different vacuum conditions.

Fabrication conditions	Contact angle with water on PVP
Low vacuum	20°
High vacuum	35°

with 150 nm ITO (15 Ω/sq) layer as the gate electrode. The cross-linked poly-4-vinylphenol dielectric layer is prepared from a solution of PVP (MW ~25,000) and poly(melamine-*co*-formaldehyde) (PMCF) in propylene glycol monomethyl ether acetate (PGMEA) with the ratio of 1:0.5:10 and is deposited via spin-coater with 3000 rpm for 60 s as described in [11]. The final thickness of the gate dielectric is 100 nm with a unit capacitance of 27–30 nF/cm^2. Then different batches are baked in the low (1.33 Pa) and high (1.33×10^{-4} Pa) vacuum condition at 160 °C [11,22–24] for 6 h. After that a 50 nm high purity pentacene (sigma, Aldrich, 99.9 + % purity) layer is thermally deposited as the conducting channel at a rate of 0.1–0.5 Å/s under a vacuum of 1.33×10^{-4} Pa. 50 nm Au source–drain electrodes are patterned through shadow mask to form the contact pad, defining the channel length (L) and width (W) of 50 μm and 500 μm respectively. The electrical characteristics are measured by means of current source meter (Keithley 2636) with an indigenous probe station. A more detailed description of the setup is provided elsewhere [25]. The surface morphology is analyzed by a Park System XE–70 non-contact mode AFM in atmospheric environment. The change in surface energy of PVP on ITO is confirmed by measuring the contact angles of water.

3. Measurements, results & discussion

Typical electrical characteristics of the pentacene based polymer dielectric are measured and plotted as shown in Fig. 2. The output characteristics for two different vacuum conditions are shown in Fig. 2(a). The field effect behavior is observed when a gate bias of the order of −1 V to −4 V are applied. This indicates the formation of the p–channel as a result of charge accumulation layer. It can also be observed that the devices with PVP baked at high vacuum have high drain current in comparison to that of low vacuum devices. Hence one can control the device performance by altering the baking condition of the polyvinyl phenol dielectric in pentacene based transistor. The transfer characteristics for each of the baking environment is presented in Fig. 2(b). The gate voltage is swept from OFF–ON state from 10 V to −20 V at 0.5 V step, while the drain source voltage is maintained at −5 V. The saturation mobility (μ_{sat}) is extracted from the slope of the square root of the drain current versus gate voltage (Fig. 2(c)) using Eq. (1), which is given by

$$I_{D,sat} = \frac{W}{2L} C_i \mu_{sat} (V_G - V_T)^2 \quad (1)$$

where $I_{D,sat}$ is the drain to source saturated current, W/L is the channel width to length ratio, C_i is the capacitance of the insulator per unit area, V_G and V_T are the gate voltage and threshold voltage respectively.

The square root of the drain current versus gate voltage curves are shown for both the vacuum conditions. The mobility, on–off ratio and the threshold voltages measured for the two conditions are presented in Table 1.

It is very much evident from the electrical characteristics and the data in Table 1 that the baking of PVP thin film at high vacuum condition enhanced the mobility, the on–off ratio and the threshold voltage considerably. All these measurements are performed on an average of 10 devices during one fabrication process in order to obtain reliable and reproducible data. As already mentioned, the surface energy of the polymer dielectric is controlled by baking the dielectric polyvinyl phenol at two different vacuum conditions. This significantly increased the field effect mobility. The change in surface energy of the gate dielectric can result in the change of orientation of the pentacene molecule [9]. Water contact angle measurement of the PVP layer on ITO/glass substrate is performed to observe the change in surface energy of PVP layers deposited at varied vacuum conditions. The corresponding data are presented in Table 2. It can be observed that with increased vacuum, the contact angle increases and hence the surface energy diminishes (Fig. 3).

The increase of mobility by 3 orders of magnitude with contact angle has already been reported in the literature [26]. But there the absolute value of mobility reported was 10^{-2}–10^{-1} cm^2/Vs. In this piece of work, the enhanced mobility is 2.02 cm^2/Vs, which is claimed to be the highest reported till date for such kind of configuration. Kim et al. [27] claimed that water molecules in humid air diffuse into the grain boundaries of the polycrystalline semiconducting layer and/or the interface between the semiconductor and gate dielectric. This severely

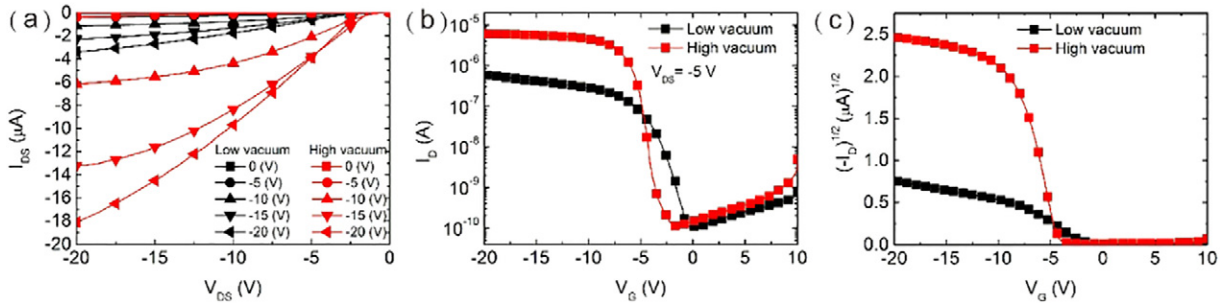

Fig. 2. Electrical characteristics of (a) output current, (b) transfer current, and (c) the square root of the drain current versus gate voltage for pentacene based OFET with PVP gate dielectric.