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Microelectronics Journal 38 (2007) 1233–1237

Microelectronics Journal

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High doped MBE Si p–n and n–n heterojunction diodes on 4H-SiC

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Received 12 July 2007; accepted 18 September 2007
Available online 29 October 2007

Abstract

The physical and electrical properties of heavily doped silicon ($5 \times 10^{19}\,cm^{-3}$) deposited by molecular beam epitaxy (MBE) on 4H-SiC are investigated in this paper. Silicon layers on silicon carbide have a broad number of potential applications including device fabrication or passivation when oxidised. In particular, Si/SiC contacts present several atractive material advantages for the semiconductor industry and especially for SiC processing procedures for avoiding stages such as high temperature contact annealing or SiC etching. Si films of 100 nm thickness have been grown using a MBE system after different cleaning procedures on n-type (0 0 0 1) Si face 8° off 4H-SiC substrates. Isotype (n–n) and an-isotype (p–n) devices were fabricated at both 500 and 900 °C using antimonium (Sb) or boron (B), respectively. X-ray diffraction analysis (XRD) and scanning electronic mircorscope (SEM) have been used to investigate the crystal composition and morphology of the deposited layers. The electrical mesurements were performed to determine the rectifiying contact characteristics and band offsets.

Keywords: Silicon carbide; Silicon; Heterodiodes; High doping Si; Rectifying contact

1. Introduction

Silicon carbide (SiC) is the best-situated semiconductor material for the next generation of power electronic devices due to its advantageous material properties, its native thermal oxide and the maturity of SiC process technology [1]. Power rectifies have become the first commercially available power device based on SiC, with several manufacturers currently supplying SiC power diode products [2,3]. Prototype SiC JFETs and BJTs are available from SiCED [4] and United Silicon Carbide Inc. [5]. However, there still remain severe technologic problems for bipolar and metal-oxide-semiconductor (MOS) gated power devices [6]. Intensive investigations are presently being carried out to overcome these problems and in parallel innovative Si/SiC co-packaging solutions such as Si IGBT/SiC Shottky diodes co-packaged or Si/SiC cascade electronic switches are being simultaneously commercialised [2]. A further step of co-packaging would be the monolithic integration of silicon and silicon carbide devices. This monolithic integration of Si and SiC devices should be considered as an attractive solution in itself for devices or even for smart power integrated circuits with the control part implemented in silicon. Although intensive investigation has been performed on epitaxial SiC layer growth on Si, the high difference in the lattice constants between Si and SiC [6] has prevented their further development. Nevertheless, for some applications such as the co-packaging of switches, even silicon layers with a relatively poor crystalline layer structure are suitable for devices [7,8]. Additionally, the formation of a silicon contact on SiC presents several technological advantages such as the inherent contact stability and the fact that the processes used to form these contacts are straightforward and commonly used by the semiconductor industry. This last advantage is especially relevant since it can simplify the fabrication of several SiC power devices avoiding stages as high temperature contact annealing or etching of SiC. In this paper, current properties and barrier heights were

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0026-2692/$ - see front matter © 2007 Elsevier Ltd. All rights reserved.
doi:10.1016/j.mejo.2007.09.019

found using analysis of the heterojunction. X-ray diffraction analysis (XRD) and scanning electronic mircorscope (SEM) have been used to investigate further the crystal composition and morphology of the deposited layers.

2. Experimental details

Silicon films have been deposited using a V100S molecular beam epitaxy (MBE) system on n-type (0 0 0 1) Si face 8° off axis 4H-SiC substrates with an epitaxial layer of 10 μm (SiC $N_{D,SiC} = 1 \times 10^{15}\,cm^{-3}$) purchased form CREE Inc. The ex-situ cleaning procedures prior to deposition are based on a standard RCA wafer cleaning processes [9]: (1) RCA2 (H_2O:HCl:H_2O_2) followed by HF dip, (2) RCA1 (H_2O:NH_4OH:H_2O_2) along with RCA2 followed by HF dip after each step and (3) piranha (H_2SO_4:H_2O_2) followed by HF dip. Once in the MBE system, an in-situ high T cleaning procedure was carried out on all the samples. Highly doped silicon n-type layers have been grown (rate of 0.1 Å/s) with doping concentration of $N_{D,Si} = 5 \times 10^{19}\,cm^{-3}$, using antimonium (Sb) as dopant at 500 and 900 °C. Analogously, highly doped silicon p-type layers have been grown ($N_{A,Si} = 5 \times 10^{19}\,cm^{-3}$) using boron (B) at 500 and 900 °C. The back contact has also been formed utilising the MBE system to form a highly doped Si(Sb) layer. The crystal structure of Si thin films was determined by XRD. The surface topology was investigated by SEM. The electrical properties (*I–V* and *C–V*) were extracted from the fabricated heterojunction diodes using both, a mercury probe and a probe station after patterning (Al). The use of a mercury probe allows very accurate lateral *C–V* measurements for determining the built-in potential of the heterojunction. *C–V* and *I–V* measurements were performed using an Agilent B1500A semiconductor parameter analyser at room temperature.

3. Results and discussion

3.1. Physical characterisation

XRD analyses reveal Cubic Si crystalline (c-Si) peaks in the θ–2θ scans on n-type 4H-SiC substrates (Fig. 1) for all the deposition conditions considered. The three main reported [10] peaks are evidenced for all the samples corresponding to c-Si(1 1 1), c-Si(2 2 0) and c-Si(3 1 1). No other impurities or composites are present. No significant differences in the XRD spectra for samples with different ex-situ pre-deposition cleaning procedures have been detected. No significant differences in the XRD spectra between n–n and p–n have been detected. Nevertheless, narrower and more intense peaks (larger crystalline grains) are achieved for Si deposited at 900 °C.

On the thin deposited MBE films, we observe that the surface roughness increases when the deposition temperature is increased due to Si grains faceting as is shown in Fig. 2. During the epitaxial growth atoms are free to move

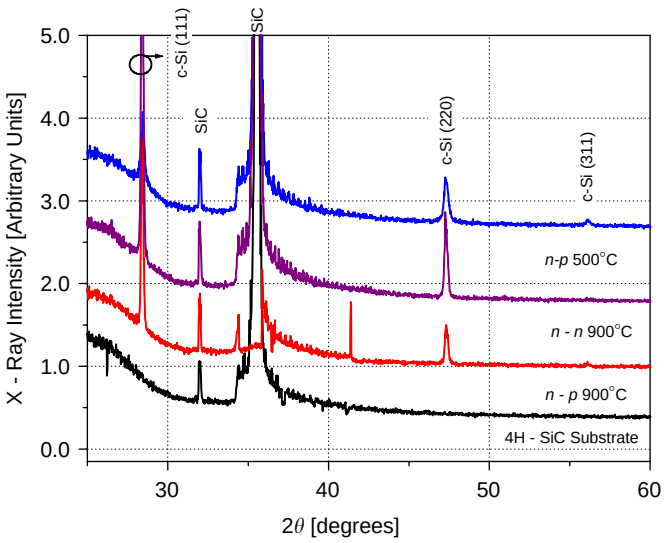

Fig. 1. XRD peaks of the MBE Si layers grown on 4H-SiC.

around on a clean surface until they find a correct position in the crystal lattice to bond. Growth occurs preferentially at the step edges since at an edge an atom experiences more binding forces than on the free surface. In practice, more than one nucleation site will exist on the surface and hence growth is by the spreading of islands. In high quality materials these islands will be large with height differences of less than a monolayer. The mobility of an atom on the surface will be greater at higher substrate temperatures resulting in smoother interfaces, but higher temperatures also lead to a lower sticking coefficient and more migration of atoms within the layers already grown. However, it is well reported that the isostructural lattices of Si and 4H-SiC presents a high mismatch [6] that leads to a strain induced surface roughening of the Si layer during growth. Si atoms would preferentially incorporate in the peaks as this is energetically favourable for the partial relaxation of the lateral strain [11]. The islands formation is then mostly based on a growth mode transition from an initial layer-by-layer to an island growth mode enhanced when increased the temperature [12] which means that the time for incorporation of the adatoms into the formed islands is shorter that the time to deposit a monolayer.

3.2. Electrical characterisation

As stressed before, high doped MBE silicon layers can be considered as an attractive procedure for the formation of ohmic contacts to SiC avoiding some steps in the fabrication process such as the high temperature annealing of the metals commonly used (Al, Ni or Ti) [13]. The effectiveness of the Si back contact on SiC is investigated with Schottky diodes using a mercury probe without further metalisation as shown in Fig. 3. The Schottky contact *I–V* obtained without any back metalisation is included for comparison (4H-SiC). As inferred from Fig. 3,