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Effects of fabrication method on defects induced by nitrogen diffusion to the hafnium oxide layer in metal–oxide–semiconductor field effect transistors

Ying-Hsin Lu [a], Ting-Chang Chang [a,c,*], Szu-Han Ho [b], Ching-En Chen [b], Jyun-Yu Tsai [a], Kuan-Ju Liu [a], Xi-Wen Liu [a], Chien-yu Lin [d], Tseung-Yuen Tseng [b], Osbert Cheng [e], Cheng-Tung Huang [e], Wei-Ting Yen [e]

[a] *Department of Physics, National Sun Yat-Sen University, Kaohsiung 804, Taiwan*
[b] *Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan*
[c] *Advanced Optoelectronics Technology Center, National Cheng Kung University, Tainan 701, Taiwan*
[d] *Department of Photonics, National Sun Yat-Sen University, Kaohsiung 804, Taiwan*
[e] *Device Department, United Microelectronics Corporation, Tainan, Science Park, Taiwan*

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This study investigates how different metal gate fabrication methods induce variations in the defects which result from nitrogen diffusing into the hafnium oxide layer in metal–oxide–semiconductor field effect transistors (MOSFETs). By using the different fabrication methods of pre-TaN, post-TaN and post-TiN annealing, the work-function difference between the gate material and the semiconductor can be adjusted, leading to apparent differences in threshold voltage (V_{th}). In addition, the results of slow and fast I–V NBTI measurements show that the amount of the bulk trapping in the post-TiN device is the highest, followed by the post-TaN device and then the pre-TaN device. In addition, a nitrogen interstitial defect phenomenon, resulting in a temporary shift of threshold voltage (V_{th}) which is highest in the post-TiN the lowest in the pre-TaN device, is determined by double sweep fast I–V measurements.

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1. Introduction

Recently, different kinds of devices such as thin-film transistors, memory devices [1–5], and IC circuits have been combined in advanced electronic products. However, with the continuous scaling down of these devices, the thickness of conventional SiO_2-based dielectric has achieved that of only a few atomic layers, resulting in increases in gate leakage current and power consumption as well as performance degradation. In order to solve this issue, high-k dielectrics such as zirconium oxide, aluminum oxide, and hafnium oxide (HfO_2) have been introduced as a replacement for conventional SiO_2 gate insulators, with the most commonly used in CMOS technology being HfO_2. Furthermore, the drive current degradation induced by hot-carrier stress would be improved by reducing the oxide thickness. According to a previous study [6], a thinner oxide more easily traps holes and these trapped holes form a buffer region at the depletion region (near the drain side) to reduce the electric field, in turn reducing the capability for impact ionization. However, the bias temperature instability (BTI) has become a noteworthy issue because of the ultra-thin gate oxide [7]. Although nitridation technology has been shown to improve the reliability of electron injection, nitrogen also diffuses into the interface to generate defects by thermal diffusion [8]. In addition, defects may also occur in the high-k material and the interface layer in high-k/metal gate (HK/MG) devices. Moreover, there are many variables influencing defect generation in high-k bulk [9–11]. Thus, this study focuses on one of those variables, the influence of different metal gate fabrication methods on nitrogen diffusion-induced defects.

1.1. Experiment

In this paper, the HfO_2/metal gate p-channel MOSFETs (p-MOSFETs) were fabricated by 28 nm CMOS technology with gate-last process, as shown in Fig. 1. First, the high quality thermal oxide with thickness of 10 Å was grown on a (100) Si substrate as an interface oxide layer. Second, 20 Å of HfO_2 dielectric was sequentially deposited by atomic layer deposition followed by the deposition of a poly-Si dummy gate. Third, self-aligned ion implantation was performed and then activated for the source/drain at 1025 °C. After removal of the dummy gate, the process was divided into three parts: one group underwent thermal annealing in an oxygen environment *before* the TaN gate deposition (pre-TaN annealing). Another one underwent thermal annealing in an oxygen environment *after* TaN (post-TaN annealing). The last

* Corresponding author at: Department of Physics, National Sun Yat-Sen University, Kaohsiung 804, Taiwan
E-mail address: tcchang3708@gmail.com.tw (T.-C. Chang).

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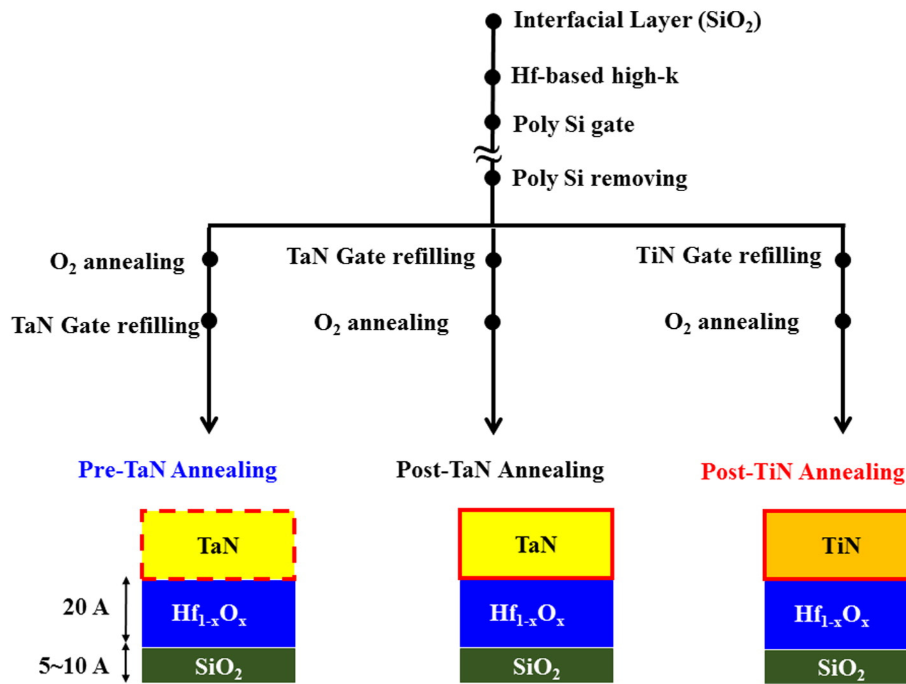

Fig. 1. The HfO_2/metal gate p-channel MOSFETs (p-MOSFETs) fabricated by gate-last process with three gate annealing processes.

underwent thermal annealing in oxygen environment after TiN (post-TiN annealing). In this study, the dimensions of the device were width/length = 500/60 nm. The NBTI for slow I–V and fast I–V measurements (slow I–V and fast I–V NBTI) were measured over a range of 30 °C to 120 °C with constant gate voltage (V_g) = V_{th} − 1.4 V with source, drain, and body terminals all grounded. The stress and recover times were both 500 s. During slow I–V NBTI, I_d–V_g curves were measured with constant drain voltage of 50 mV, and the integration time was a few ms. During fast I–V NBTI, I_d–V_g curves were measured using fast I–V with an integration time of 7×10^{-6} s, a step edge of 5×10^{-7} s, and step number of 10. For the analysis of process-related pre-existing defects, I_d–V_g curves were measured by fast I–V technology in double sweep modes of fixed base level voltage ($V_{base\ level}$) and various high level voltages ($V_{high\ level}$), with constant drain voltage of 50 mV, an integral time of 5×10^{-6} s, a step edge of 1×10^{-8} s, and step number of 10. In addition, the hold time and delay time were both 5 s in order to ensure the steady state of devices in $V_{base\ level}$ and $V_{high\ level}$. All experimental results were measured using an Agilent B1530 semiconductor parameter analyzer and a Cascade M150 probe station.

2. Results and discussion

Comparisons of initial electrical characteristics of V_{th}, subthreshold swing (S.S.), and gm_{max} for ten randomly chosen pre-TaN and

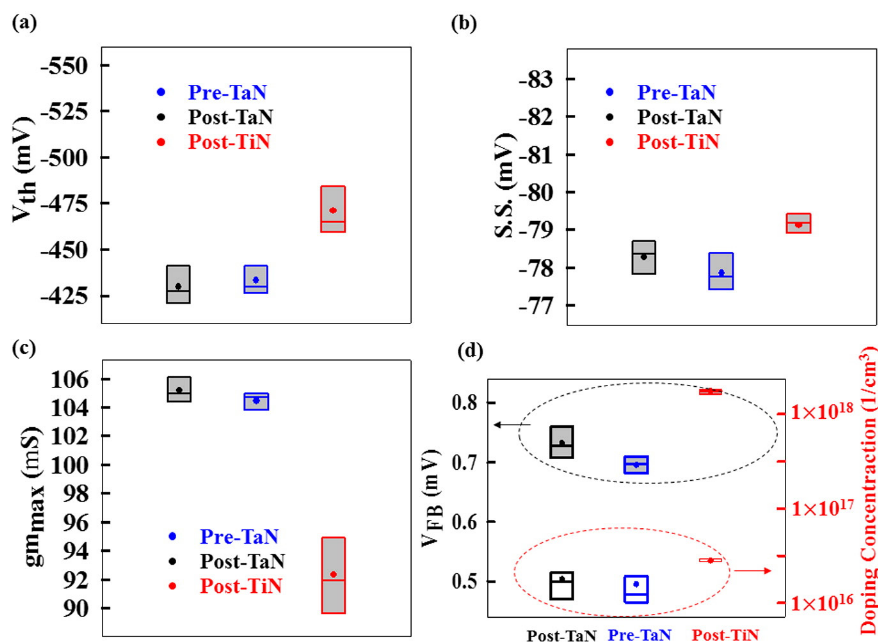

Fig. 2. Comparisons of initial electrical characteristics of five randomly chosen devices for each annealing process (fifteen total). (a) V_{th}, (b) subthreshold swing, (c) gm_{max}, and (d) the results of N_A and V_{FB}.

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