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High mobility thin film transistors based on zinc nitride deposited at room temperature

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ABSTRACT

In this work, the characterization of high mobility thin-film transistors based on zinc nitride films deposited at room temperature by magnetron radio-frequency sputtering is presented. The values extracted of field-effect mobility were $>2 \text{ cm}^2/\text{Vs}$ for long channel devices. For short channel devices, a reduction of the mobility values is found and, as a result of the analysis of the width-normalized resistance for different channel lengths and gate voltages, the reduction is attributed to the effects of a high contact resistance. The impact of the gate dielectric thickness on electrical characteristics is also presented.

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1. Introduction

Currently, many semiconductor materials, such as metal-oxide, organic and chalcogenide semiconductors, are attracting a great deal of interest to become active materials of advanced thin-film transistors (TFTs) that enable the development of flexible electronics [1–4]. However, the low-temperature deposition necessary to fabricate the TFTs in flexible substrates severely restricts the field-effect carrier mobility of traditional semiconductors. Since several works reported Hall mobilities above $80 \text{ cm}^2/\text{Vs}$, Zn_3N_2 films have been proposed as active layers in TFTs in order to achieve high electron mobilities at low temperature of deposition [5–7]. A previous work identified the optical properties of this semiconductor, which had remained in controversy [8]. At the surface of this film, oxidation tends to form a ZnO native film whose thickness increases over time. For this reason, in this work, ZnO was used as passivation layer to reduce the oxidation of the Zn_3N_2 films. In this work, the characterization of high mobility TFTs based on Zn_3N_2 films deposited at room temperature is presented. The effects of a high contact resistance on the electrical characteristics are studied. The impact of the gate dielectric thickness on electrical characteristics is also presented.

2. Experiment

The Zn_3N_2 films were plasma sputtered at room temperature. The plasma discharge was induced between a 4 in. circular Zn target (99.995% purity) and the substrate, using 30 sccm flux of Nitrogen gas (99.999%) with a radio frequency power of 100 W. The base and working pressures are 10^{-5} mbar and 10^{-2} mbar, respectively. To avoid Zn_3N_2 oxidation, a ZnO thin film was plasma sputtered at room temperature from the same Zn target using 50 sccm flux of Oxygen gas (99.999%) and a radio frequency power of 250 W. The plasma sputtered system used was the A450 ALCATEL model.

Crystallinity was studied using grazing incidence X-ray diffraction (XRD) in a Siemens D-5000 (Cu $\text{K}\alpha 1$) system at 2θ values between 20° and 80° . In this configuration, the grazing angle (0.5°) is such that the total reflection condition is satisfied and the X-rays are totally reflected. Under this condition, the evanescent wave is diffracted by sets of crystal planes that are perpendicular to the sample surface and depth penetration is limited. Substrate signals are therefore eliminated and the diffraction pattern only contains Bragg reflections from the surface layer.

To fabricate the inverted coplanar Zn_3N_2 TFTs (bottom-contact bottom-gate), the passivated active layer (20 nm-thick ZnO atop 20 nm-thick Zn_3N_2) was deposited over 100 nm-thick aluminum electrodes (e-gun evaporated) patterned on thermally grown SiO_2 on heavily doped Si wafers. The heavily doped Si wafer was used as the gate electrode. Fifty (50) nm and 100 nm-thick thermally grown SiO_2 were used to compare the effects of the gate dielectric thickness. The Zn_3N_2 TFTs were fabricated with different channel lengths L from 5 to 30 μm and one channel width W of 120 μm only. The electrical characteristics

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were measured using the Keithley-4200 Semiconductor Characterization System, under dark conditions, air ambient and room temperature.

3. Results and discussion

Fig. 1 shows the XRD pattern of the Zn_3N_2 film deposited at room temperature. The Zn_3N_2 film shows three peaks at $2\theta = 36.9^\circ$, 52.98° and 62.98° which are associated to the (400), (440) and (622) planes. From the overall XRD diffractogram the Zn_3N_2 film presents a polycrystalline structure. The film deposited exhibits a preferred orientation to the (400) plane, which has been associated to high quality Zn_3N_2 films deposited at higher temperatures [5,6].

Fig. 2 shows the comparison of the transfer characteristics of Zn_3N_2 TFTs with 50 nm and 100 nm-thick gate dielectrics. Higher on-current, higher on/off-current ratio and better subthreshold region are found for TFTs with 50 nm-thick gate dielectric. The improvement in transfer characteristics is associated to a higher transconductance in the device by the thinner gate dielectric, since the transconductance g_m is proportional to the oxide capacitance C_{ox} of the device as shows Eq. (1) [2].

$$g_m = (\mu_{FE} C_{ox} W/L) (V_{gs} - V_T) \quad (1)$$

where μ_{FE} is the field-effect mobility, C_{ox} is the capacitance per unit area of the gate dielectric, W and L are the channel width and the length, respectively, and V_T is the threshold voltage.

Fig. 3 shows the normalized transfer characteristics of the Zn_3N_2 TFTs with 50 nm-thick gate dielectric for 5 and 30 μm channel lengths. The on/off current ratio $> 10^2$ and subthreshold slope ($> 7 \text{ V/Dec}$) are unexpected values. Moreover, the normalized off- and on-currents decrease for TFTs with short channel length L (5 μm). These are attributed to contact effects resulted by a high contact resistance [9].

The electron field-effect mobility and threshold voltage were extracted from the square root of I_{ds} versus V_{gs} , using the Eq. (2) of the saturation regime [10].

$$I_{ds} = \mu_{FE} \cdot C_{ox} (W/2L) (V_{gs} - V_T)^2 \quad (2)$$

where μ_{FE} is the electron field-effect mobility, C_{ox} is the capacitance per unit area of the gate insulator, W and L are the channel width and length, respectively, and V_T is the threshold voltage. The values extracted for threshold voltage V_T were in the range of -11.07 to -9.53 V .

Fig. 4 shows the field-effect mobility extracted at different channel lengths. The extracted values for TFTs with channel lengths $L > 5 \mu\text{m}$

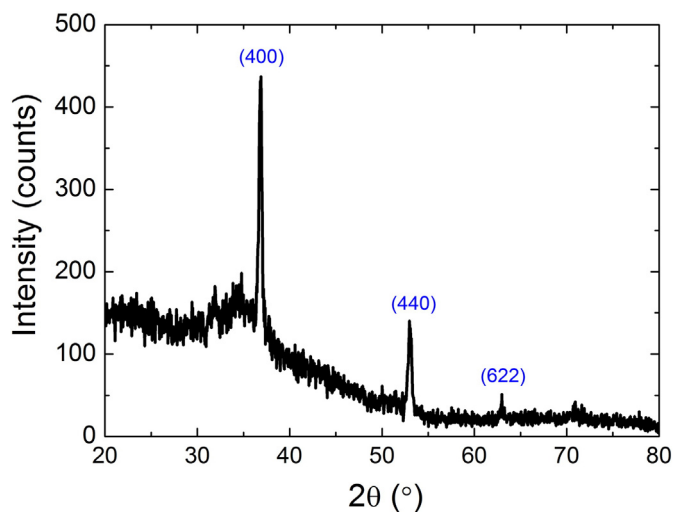


Fig. 1. XRD pattern of the Zn_3N_2 film deposited at room temperature. The Zn_3N_2 film shows three peaks at $2\theta = 36.9^\circ$, 52.98° and 62.98° which are associated to the (400), (440) and (622) planes.

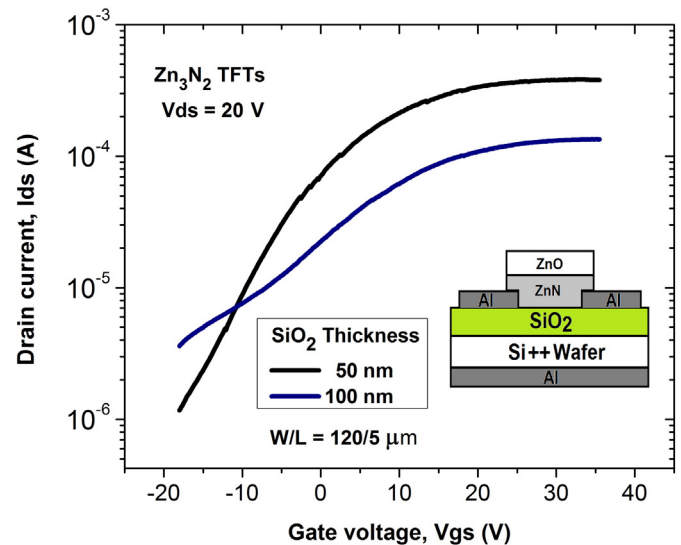


Fig. 2. Comparison of the transfer characteristics of Zn_3N_2 TFTs with 50 nm and 100 nm-thick gate dielectrics. The improvement in transfer characteristics corresponds to a higher transconductance in the device by the thinner gate dielectric.

present approximately similar values; however, for TFTs with short channel length ($L = 5 \mu\text{m}$), the field-effect mobility drastically drops. This effect is also attributed to high contact resistance effects [11–12]. As the channel length is scaled down, the source/drain contact resistance is higher than the channel resistance, then, the contact resistance tends to dominate the electrical characteristics of the device. In particular, a high contact resistance may induce several mechanisms such as current crowding, degradation of the transconductance, or impact ionization, among others [9,11,13–15].

In order to corroborate the high contact resistance, the contact resistance was extracted from the Zn_3N_2 TFTs by the extrapolation of the width-normalized resistance (RW) (obtained from the linear regime of I_{ds} vs V_{ds}) for different channel lengths and gate voltages V_{gs} , as indicated in Fig. 5 [16].

The $2RcW$ obtained was approximately $959.9 \Omega \text{ cm}$, where higher values than $200 \Omega \text{ cm}$ are considered as high contact resistance [17–19]. This high contact resistance may be due to an ultrathin native Al_2O_3 layer formed in the metal-semiconductor interface [20]. The

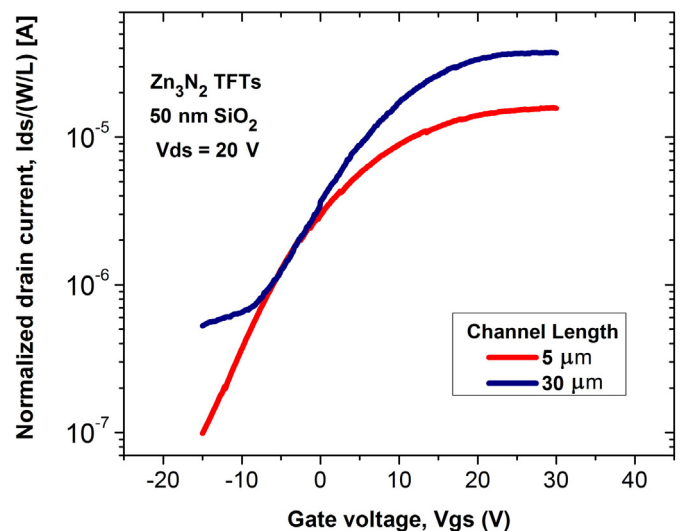


Fig. 3. Normalized transfer characteristics of the Zn_3N_2 TFTs with 50 nm-thick gate dielectric for 5 and 30 μm channel lengths. The off- and on-current decrease for TFTs with short channel length L (5 μm) due to high contact resistance effects.

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