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Temperature dependence of charge transport in zinc oxide nanosheet source-gated transistors

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ABSTRACT

In the present work, we report the high performance of zinc oxide (ZnO) nanosheet (NS) based source-gated transistors (SGTs) with asymmetric Schottky source and ohmic drain contacts: low saturation drain-source voltages (~2 V) in the output scans (even at high gate voltages), high current on/off ratio (>10^7) and low off-currents (0.1 pA). For a deeper understanding of the device mechanism and charge transport at metal–semiconductor contact interface, temperature dependent current–voltage studies have been performed. They revealed that the device operation can be ascribed to 3 main processes: i) the reverse biased Schottky source contact, which essentially controls charge carrier injection in to the NS channel, ii) effective manipulation of the source barrier by the gate field and iii) modulation of the depletion region beneath the source contact. These results are likely to improve the future generations of the ZnO based SGTs which offer several advantages for thin-film transistor design, including low power dissipation, small signal amplification, and as active load for the electronic circuits.

1. Introduction

Reducing power consumption in integrated circuits is a key issue to address for the realization of high performance low-power electronics. One possible solution to achieve this goal is to design low powered transistors, which currently represents the basic building blocks for nearly all electronic systems. Combining bottom-up approaches with the existing conventional microfabrication techniques has ignited significant research interest in this area for developing functional thin-films and nanomaterials [1–3]. The field of search has led to many demonstrations of nanoscale field-effect transistors (FETs) incorporating semiconducting nanostructures such as carbon nanotubes [4,5], nanowires [3,6], and more recently, single atomic layer of metal dichalcogenides [2]. Among the various transistor configurations [1–3], source-gated transistors (SGTs) offer several attractive features that are currently unobtainable with conventional transistors [1,6–15].

SGT is a three terminal device, like a standard FET, but with a Schottky barrier at the source contact instead of an ohmic one. The portion of the active semiconductor element which forms the Schottky junction is also sandwiched between the source electrode and the gate insulator. Fig. 1 shows a typical cross-sectional view of the SGT device structure. Unlike conventional FETs, the SGT exploits the reverse biased Schottky barrier at the source to afford much lower saturation voltages even at high gate voltages (V_G) [1]. This unique feature of the device ensures that drain current (I_D) progression with the drain voltage (V_D) is dominantly controlled by the reverse bias source contact and not by the active semiconductor channel (if the applied V_D is large enough to deplete the entire channel). This effect leads to several advantages compared to FETs, including extremely early drain current saturation (I_D^{SAT}), low output conductance, invariant with V_D variations beyond the saturation voltage (V_D^{SAT}), and stable operation with prolonged gate bias stress. The device also offers potential immunity to short-channel effects. To date, SGT device structures have mainly been realized from amorphous and polycrystalline silicon [15] [7] and polycrystalline zinc oxide (ZnO) thin-films [8].

With many distinctive advantages of SGTs, such as, low saturation voltage, high output impedance in saturation, and high tolerance to electrical stress, compared to conventional FETs, one parameter that delimits the performance of SGTs is temperature dependence of charge transport. Due to the contact controlled characteristics, SGT exhibits strong positive temperature dependence charge transport. Therefore, current may increase with temperature and thus the device performance can be changed. Although there are few reports on temperature dependent performance of SGTs based on thin-film technology [10,16,17], no such investigations are being reported on SGTs based on nanostructure(s). Among the various semiconducting nanostructures, ZnO exhibits a number of unique electrical and optical properties such as wide band-gap (3.34 eV), high exciton binding energy (60 meV), excellent thermal stability, and high carrier mobility (~200 $cm^2 V^{-1} s^{-1}$).

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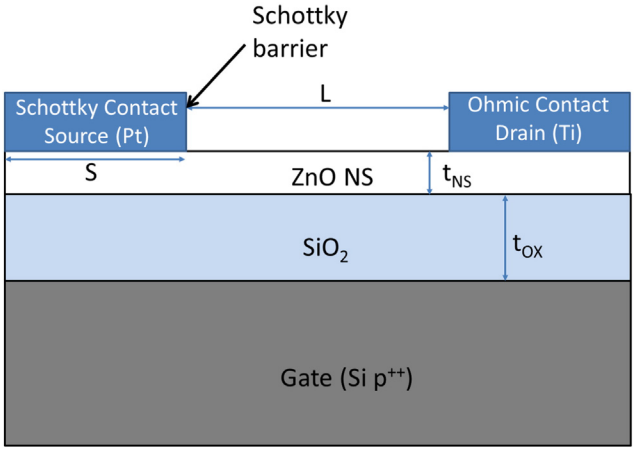

Fig. 1. Schematic of the SGT device structure (L = separation gap between source and drain, S = source contact length, t_{NS} = ZnO nanosheet thickness, and t_{OX} = silicon oxide thickness).

Furthermore, the relative ease in synthesizing plethora of ZnO's nanostructures [18] provides researchers ample scope to realize nanoscale devices using ZnO nanostructures [19].

In this work, we will demonstrate the growth of high quality single-crystalline ZnO nanosheets (NSs) on Au coated r-Sapphire substrate using vapour–liquid–solid (VLS) approach in a conventional horizontal tube furnace. These ZnO NSs can be considered as two-dimensional single-crystalline thin-films. Then, we will show the successful incorporation of ZnO NS for the fabrication of fully functional SGTs and the SGT device performance will be compared with an identical device with ohmic contacts (FET). Lastly, temperature-dependent charge transport measurements will be performed on SGTs and detailed discussions concerning device performance will also be given.

2. Experimental section

High density of single-crystalline ZnO NSs has been synthesized by a conventional VLS process using a horizontal tube furnace on Au-coated r-Sapphire substrates at 900 °C, similar to the method reported before [20]. Fig. 2a shows the schematic of the VLS growth process which we employed for ZnO NS synthesis. The source material (ZnO and carbon at 1:1 weight ratio) and Au-coated r-Sapphire were placed in an Alumina boat, which was subsequently inserted close to the centre of the quartz tube furnace. An Ar ambient, with a constant flow rate of 700 sccm (standard cubic centimetres per minute), was maintained inside the growth chamber throughout the growth process, and no vacuum systems were employed during growth. To initiate the growth, tube furnace was ramped to 900 °C at a ramp rate of 30 °C min^{-1}, while the growth time at the plateau (900 °C) was varied from 60 to 180 min, depending on the desired length of the NSs. After the growth, the furnace was switched off and left to cool down naturally to room temperature and growth substrates were recovered thereafter. To assess the morphological and structural characterizations, NSs were analysed by scanning electron microscopy (SEM) and high resolution transmission electron microscopy (HRTEM). For SEM imaging, a dual beam FEI Strata 400 (FEI, Hillsboro, OR, USA), a focused ion beam (FIB) coupled to a SEM system, has been used at an operating voltage of 10 kV. The HRTEM characterizations were performed using a JEOL 2100 F, operating at an accelerating voltage of 200 kV. For HRTEM analysis, samples were prepared by drop-casting NS formulation, in isopropanol, over the TEM grids (Agar scientific, AGS162-3).

To fabricate the ZnO NS SGT devices, as-grown ZnO NSs were dispersed onto highly doped Si substrate with 170 nm thick thermally grown silicon oxide (SiO_2). Metallic source/drain (s/d) contacts on to the opposite ends of a selected NS are defined using a two-step electron-beam lithographic process. In contrast to conventional FETs (ohmic contacts), the SGTs have a Schottky source contact. This is achieved, using high work function metal (Pt) during the first lithography step. Accordingly, an ohmic drain contact is defined using low work

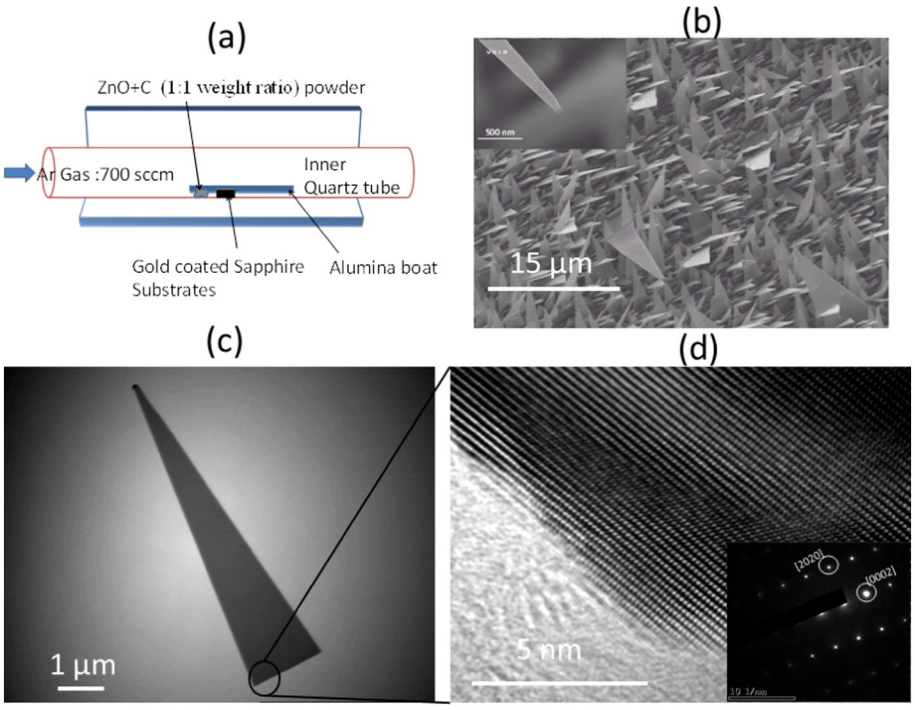

Fig. 2. (a) Schematic of the VLS growth process carried out in a horizontal tube furnace. (b) SEM image of the as-grown ZnO NSs on r-plane sapphire substrate. The inset is high-magnification image of the respective sample. (c) Low magnification HRTEM image of single ZnO NS showing the region scanned for high magnification HRTEM. (d) High magnification HRTEM image of ZnO NS. The inset selected area electron diffraction (SAED) pattern further confirms the single crystalline nature of the NS.

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