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Voltage optimization for simultaneous energy efficiency and temperature variation resilience in CMOS circuits ☆

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Abstract

A design technique based on optimizing the supply voltage for simultaneously achieving energy efficiency and temperature variation insensitive circuit performance is proposed in this paper. The supply voltages that suppress the propagation delay variations when the temperature fluctuates are identified for a diverse set of circuits in 180 and 65 nm CMOS technologies. Circuits display temperature variation insensitive propagation delay when operated at a supply voltage 44–47% lower than the nominal supply voltage ($V_{DD} = 1.8$ V) in a 180 nm CMOS technology. Similarly, the optimum supply voltages are 67–68% lower than the nominal supply voltage ($V_{DD} = 1.0$ V) in a 65 nm CMOS technology. At scaled supply voltages, integrated circuits consume lower power at the cost of reduced speed. The proposed design methodology of optimizing the supply voltage for temperature variation insensitive circuit performance is, therefore, particularly attractive for low-power applications with relaxed speed requirements. A new design methodology based on threshold voltage optimization for achieving temperature variation insensitive circuit speed is also evaluated. The energy per cycle and the propagation delay at the supply and threshold voltages providing temperature variation insensitive circuit performance, minimum energy-delay product, and minimum energy are compared. Results indicate that low-power operation and temperature variation tolerance can be simultaneously achieved with the proposed techniques.

Keywords: Minimum energy; Minimum energy-delay product; Propagation delay fluctuations; Supply voltage optimization; Temperature variations; Threshold voltage optimization

1. Introduction

Process and environment parameter variations in scaled CMOS technologies are posing greater challenges in the design of reliable integrated circuits. Because of the unbalanced utilization and diversity of circuitry at different sections of an integrated circuit, temperature can vary significantly from one die area to another [1]. Furthermore, environmental temperature fluctuations can cause significant variations in die temperature. For example, electronic systems mounted on automobile engines operate at a temperature range from −40 to 150 °C [2,3]. Temperature variations affect the device characteristics of MOSFETs thereby varying the performance of integrated circuits.

The supply and threshold voltages are scaled with each new technology generation. The supply voltage is scaled primarily based on the device reliability and target clock frequency requirements in a new technology generation. Scaling the device dimensions strengthens the electric fields between device terminals while lowering the parasitic capacitances, thereby increasing the speed of CMOS integrated circuits. The speed of a circuit can be further enhanced by scaling the threshold voltages. Due to the subthreshold leakage current constraints, however, the threshold voltages are scaled at a much slower rate as compared to the supply voltage. The supply voltage to threshold voltage ratio is reduced with each new technology generation. The temperature fluctuation induced threshold voltage variation is therefore expected to have an increasingly important role in determining the

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MOSFET drain current variations when the temperature fluctuates. A complete reversal of temperature dependent speed characteristics of CMOS circuits is also likely to occur in the near future [4].

Propagation delay of a circuit is a function of the drain saturation current produced by active transistors. Temperature fluctuations alter threshold voltage, carrier mobility, and saturation velocity of a MOSFET [5,22]. Temperature fluctuation induced variations in individual device parameters have unique effects on MOSFET drain current. Performance variation of an integrated circuit under temperature fluctuations is determined by the device parameter whose variation dominates the drain current produced by the MOSFETs.

Temperature dependent device parameters that cause MOSFET drain current variations in the TSMC 180 nm and the predictive 65 nm CMOS technologies are identified in this paper. A design methodology based on optimizing the supply voltage for temperature variation insensitive circuit performance is proposed. The optimum supply voltages that achieve temperature variation insensitive propagation delay for a diverse set of circuits in 180 and 65 nm CMOS technologies are presented.

In circuits that exhibit reversed temperature dependence, the optimum supply voltages that yield temperature variation insensitive delay are higher than the nominal supply voltage [4]. Alternatively, the optimum supply voltages are lower than the nominal supply voltage in 180 and 65 nm CMOS technologies. Integrated circuits operating at scaled supply voltages consume low power at the cost of reduced speed. The design methodology of optimizing the supply voltage for temperature variation insensitive circuit performance in 180 and 65 nm CMOS technologies is, therefore, particularly attractive in low-power applications with relaxed speed requirements.

In this paper, the supply voltages that achieve minimum energy-delay product and minimum energy are identified at two different temperatures for circuits in the TSMC 180 nm and the predictive 65 nm CMOS technologies. The energy per cycle and speed at the supply voltages providing temperature variation insensitive propagation delay, minimum energy-delay product, and minimum energy are compared. An alternative method based on threshold voltage optimization for suppressing the propagation delay variations when the temperature fluctuates is also evaluated. The speed and energy tradeoffs with the two optimization techniques are compared.

The paper is organized as follows. The influence of temperature dependent device parameters on the drain current of a MOSFET is analyzed in Section 2. Effect of temperature fluctuations on the device and circuit characteristics is examined in Section 3. The optimum supply voltages providing temperature variation insensitive circuit performance are presented in Section 4. The supply voltages that yield minimum energy-delay product and minimum energy are identified in Section 5. The tradeoffs of operating the circuits at the supply voltages providing temperature variation insensitive circuit speed are discussed in Section 6. The threshold voltage optimization technique for temperature variation insensitive speed is presented in Section 7. Finally, some conclusions are given in Section 8.

2. Factors influencing MOSFET current under temperature fluctuations

Device parameters that are affected by temperature fluctuations, causing variations in the drain current produced by a MOSFET, are identified in this section. BSIM3 and BSIM4 MOSFET current equations are used for an accurate characterization of temperature fluctuation induced drain current variations in deeply scaled nanometer devices. The drain current of a MOSFET is [6–8]

$$I_{ds} \propto \frac{I_{ds0}}{1 + R_{ds} I_{ds0} / V_{dseff}}, \tag{1}$$

$$I_{ds0} \propto \frac{V_{gsteff} \mu_{eff} V_{dseff} (1 - A_{bulk} V_{dseff} / 2(V_{gsteff} + 2V_T))}{(1 + V_{dseff} / E_{SAT} L_{eff})}, \tag{2}$$

where I_{ds}, I_{ds0}, R_{ds}, V_{dseff}, V_{gsteff}, A_{bulk}, μ_{eff}, V_T, E_{SAT}, and L_{eff} are the drain current with short-channel effects, drain current of a long channel device, parasitic drain-to-source resistance, effective drain-to-source voltage, effective gate overdrive ($V_{GS} - V_t$), parameter to model the bulk charge effect, effective carrier mobility, thermal voltage, electric field at which the carrier drift velocity saturates, and effective channel length, respectively.

Threshold voltage, saturation velocity, and carrier mobility are [7,8]

$$\text{NMOS}: V_t(T) = V_t(T_0) + \left(KT1 + \frac{KT1L}{L_{eff}} + V_{bseff} KT2\right) \times \left(\frac{T}{T_0} - 1\right), \tag{3}$$

$$\text{PMOS}: V_t(T) = V_t(T_0) - \left(KT1 + \frac{KT1L}{L_{eff}} + V_{bseff} KT2\right) \times \left(\frac{T}{T_0} - 1\right), \tag{4}$$

$$V_{SAT}(T) = V_{SAT}(T_0) - AT\left(\frac{T}{T_0} - 1\right), \tag{5}$$

$$\mu_{eff}(T) = \left(U_0 \left(\frac{T}{T_0}\right)^{U_{te}}\right) \left\{1 + \left(\frac{V_{gsteff} + 2V_t(T)}{T_{OXE}}\right)^2 U_b(T) + (U_c(T) V_{bseff} + U_a(T)) \left(\frac{V_{gsteff} + 2V_t(T)}{T_{OXE}}\right)\right\}^{-1}, \tag{6}$$

where V_t, $KT1$, $KT1L$, $KT2$, V_{bseff}, U_0, U_{te}, T_{OXE}, U_a, U_b, U_c, V_{SAT}, AT, T_0, and T are the threshold voltage with short-channel effects, temperature coefficient for threshold voltage, channel length dependence of the temperature