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Power efficiency evaluation in Dickson and voltage doubler charge pump topologies

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Abstract

This paper presents a theoretical and experimental comparison between two charge pump architectures commonly used in CMOS integrated circuits, namely the Dickson scheme and the cascade of voltage doublers. The comparison is carried out considering power efficiency as the main feature of interest. To compare the two topologies, two charge pumps were integrated in 0.18-μm triple-well CMOS technology. The two charge pumps were designed with the same operating clock frequency, the same storage capacitance per stage, and the same number of stages (and, thus, approximately the same area). The theoretical and the experimental comparison showed that the power efficiency of the voltage doubler scheme is higher (by about 13% at $I_{out} = 1$ mA), mainly thanks to the lower parasitic capacitance associated to the boosted nodes.

Keywords: Charge pump; Power efficiency; Dickson; Voltage doubler

1. Introduction

The scaling down of transistor channel length and oxide thickness leads to the continuous reduction of area occupation and supply voltage (V_{DD}) in integrated circuits. In the case of digital systems, since the main contribution to the overall power loss is represented by dynamic losses (which are proportional to V_{DD}^2), the use of low supply voltage is highly desirable. Nevertheless, several devices integrating both analog and digital circuits (such as LCD displays, non-volatile memories, and smart power devices) require operating voltages higher than V_{DD} [1]. In these devices, it is therefore mandatory to integrate DC–DC voltage converters (which are generally referred to as voltage elevators), so as to generate the required high voltages from the available power supply V_{DD}. Fig. 1 shows a schematic diagram of a voltage elevator. Typically, the above mentioned devices require voltages higher than $2V_{DD}$, which is obtained by using the cascade connection of N stages ($N > 1$).

The most popular schemes for integrated voltage elevators are based on the charge pump approach [2], which is commonly used to generate both positive and negative high voltages while providing the desired current driving capability.

In the case of portable applications, minimizing power consumption is a key issue. As a consequence, one of the most relevant figures of merit of voltage elevator topologies is power efficiency, hereinafter referred to as efficiency for simplicity.

The efficiency η of a voltage elevator is defined as the ratio between the power P_{out} delivered to the load and the power P_{in} drawn from the supply V_{DD}. The input power P_{in} is equal to the sum of the output power P_{out} and the overall power losses P_{loss} and, hence, the value of η can be expressed as

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}}. \quad (1)$$

In this paper, we present a theoretical and experimental comparison between two of the most popular schemes for integrated charge pumps (i.e., the Dickson and the voltage doubler topologies). In Section 2, a basic description of the architectures and the operating principles of Dickson

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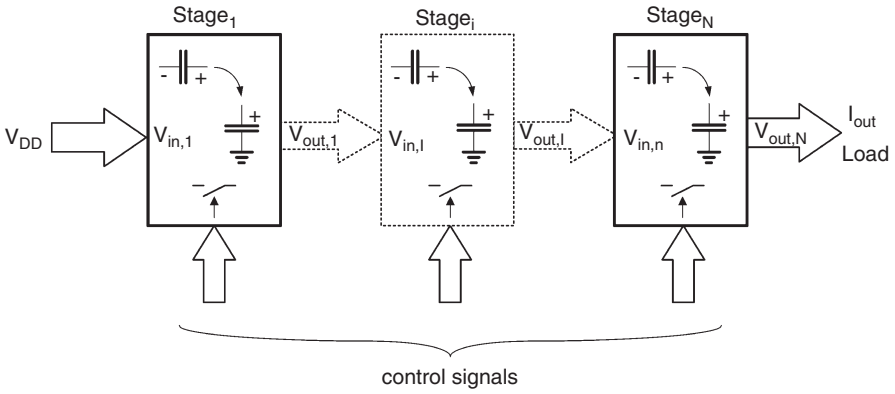

Fig. 1. Schematic representation of a voltage elevator.

topology and the cascade of voltage doublers is provided. A theoretical analysis, which points out the parameters affecting efficiency, is presented in Section 3, whereas in Section 4, efficiency comparison between the two topologies is carried out. Experimental results confirming the conclusions of the theoretical analysis are shown in Section 5.

2. Dickson and voltage doubler structures

Dickson charge pump [2–5] is widely used in mixed mode circuits, smart power ICs and non-volatile memory chips to generate the required high voltages. Two cascaded stages of a CMOS integrated Dickson scheme are shown in Fig. 2. Since the maximum voltage increment provided by a single stage is (ideally) equal to V_{DD}, a Dickson charge pump is typically obtained as the cascade connection of a suitable number N of identical stages, which ideally gives an output voltage V_{out} equal to $(N+1)\cdot V_{DD}$.

In order to generate the required high voltage, the storage capacitors $C_{DK,i}$ in the odd and the even stages are alternatively boosted by means of specific control signals. Suitable phase drivers (typically consisting of tapered chains of CMOS inverters) provide the control signals. A part of the charge stored in capacitor $C_{DK,i}$ is transferred through the NMOS switch M_{i+1} to storage capacitor ($C_{DK,i+1}$) of the next stage. This way, after an initial transient, the voltage drop across capacitor $C_{DK,i+1}$ is (ideally) higher by an amount V_{DD} with respect to the voltage drop across $C_{DK,i}$. To prevent undesired voltage drops across switch M_i (which strongly affect the voltage increment per stage), boosting circuits must be used so as to reduce the switch on-resistance [6–8]. To this end, additional switches (M'_i) and capacitors ($C_{BST,i}$) are needed. Due to the presence of boosting elements, in order to avoid undesired charge feedback, this structure requires four non-overlapping control signals [9]. In particular, ϕ_3 and ϕ_1 are used to drive pump capacitors ($C_{DK,i}$ and $C_{DK,i+1}$, respectively), whereas ϕ_2 and ϕ_4 are used to boost the gates of switches M_i and M_{i+1}, respectively, during charge transfer.

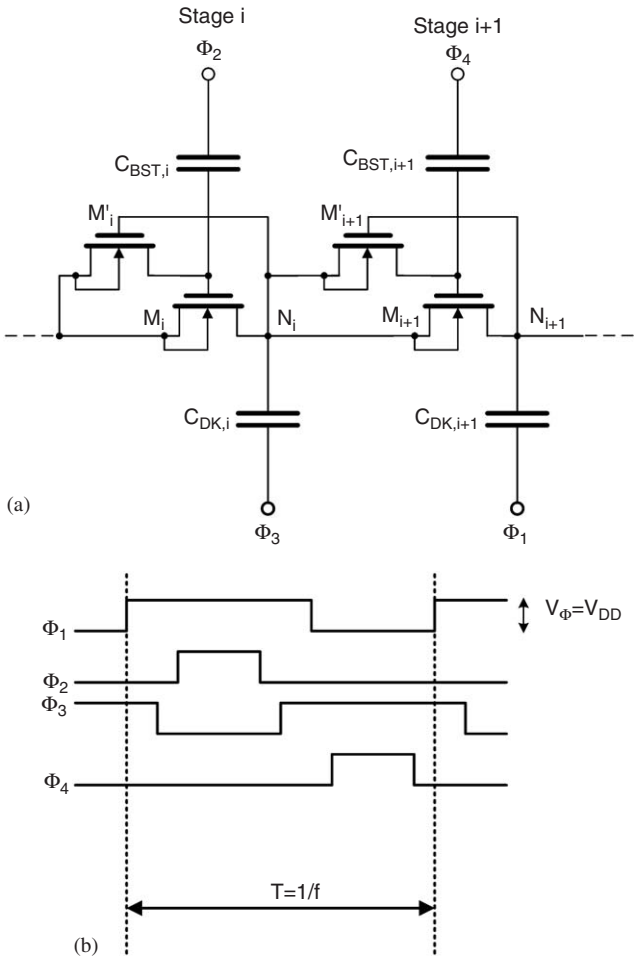

Fig. 2. (a) Two stages of a Dickson charge pump (schematic view) and (b) four-phase control signals (time delays not to scale).

To prevent excessive gate oxide stress, high-voltage transistors must be used. In fact, before and after the time interval when $C_{DK,i+1}$ supplies charge to the next storage capacitor, i.e., when $\phi_1 = V_{DD}$ and $\phi_2 = \phi_3 = \phi_4 = 0$, a voltage drop of about twice the supply voltage is applied between nodes N_{i+1} and N_i and, hence, across the gate oxide of M_{i+1} and M'_{i+1}. The main disadvantage of high voltage devices is their high threshold voltage, which leads