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Microelectronics Journal 37 (2006) 510–518

Microelectronics Journal

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Design of a Hamming neural network based on single-electron tunneling devices

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Received 13 May 2005; received in revised form 23 July 2005; accepted 27 July 2005
Available online 10 October 2005

Abstract

In this paper, the first complete implementation of a Hamming neural network based on single-electron devices is presented. A large-scale network for character recognition simulation based on building block approach was successfully carried out. Simulations were done using SIMON and MATLAB softwares. Effects such as offset charges and dynamic behavior are taken into account. Moreover, room temperature operation is considered.

PACS: 73.23HK; 84.35.+i; 85.35Gv; 85.40.−e

Keywords: Single-electron; Neural network; Room temperature; Hamming network; Block; Recognition

1. Introduction

Nanoelectronic devices [1,2] are an extremely attractive option for developing GSI (Giga-Scale Integration) or even TSI (Tera-Scale Integration) circuits [3] with dimensions and performance limits [4] beyond the last Semiconductor Industry Association's (SIA) roadmap projections [2].

Among nanoelectronic devices, single-electron tunneling (SET) devices based on tunnel junctions [1,5–7] present the following features: low power consumption, reduced dimensions and current control. These features should allow building chips with a number of devices orders of magnitude greater than the indicated by the roadmap [2] still respecting area and power consumption restrictions. In this sense, a TSI processor may be feasible in the future.

However, nanoscaled SET devices present instabilities resulting from local phenomena, like offset charges [8] and co-tunneling [9]. Such effects can degrade their electrical performance [1,10]. To overcome these limitations, parallel processing architectures, like neural networks, should be considered [3,11]. Artificial neural networks seem advantageous because of their high parallelism and redundancy. Consequently, these networks present robustness against local fluctuations [12].

Competitive neural networks, like *winner-take-all* (WTA), provide easiness of operation due their unsupervised training [13,14]. In addition, these neural networks have a reduced number of control signals, self-organization and local memory [13,15]. Usually, WTA networks are used together with another neural network layer to implement tasks such as: decision making, pattern recognition, feature extraction, image processing, video compression, Hamming network and others [16].

In the literature, some SET neurons have already been proposed. Goossens et al. [17] provided some examples of single-electron circuits for synapses and neurons. Kirihara and Taguchi [18] showed a more complex neuron circuit with n inputs and $6n+2$ SET transistors. However, both worked with supervised networks.

Yamada and Ameniya developed a SET Hopfield network [19] and a SET Boltzmann machine [20]. Nevertheless, the operation of these circuits had not considered offset charges and room temperature operation.

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[1] Janaina Guimarães acknowledges CAPES-Brazil and CNPq-Brazil for support.

0026-2692/$ - see front matter © 2005 Elsevier Ltd. All rights reserved.
doi:10.1016/j.mejo.2005.07.007

A SET winner-take-all network has already been proposed [21–23]. This network was simulated implementing a Hamming network taking into account effects such as offset charges and temperature variations. Nevertheless, the input layer was simulated mathematically, i.e. it was not implemented with nanoscaled devices.

In this paper, a Hamming neural network completely designed using SET devices is presented for the first time. A character recognition task is simulated at room temperature using building blocks [22]. Robustness against offset charges, as well as dynamic behavior are evaluated.

2. Hamming network

The Hamming network [24] is a maximum likelihood classifier for disturbed bipolar binary inputs. So, for a set of m exemplar vectors $\mathbf{e}_1^{\rightarrow}, \mathbf{e}_2^{\rightarrow}, \ldots, \mathbf{e}_m^{\rightarrow}$ it finds the exemplar which is most similar to a given input vector $\mathbf{x}^{\rightarrow}$.

A Hamming network has two neural layers, as shown in Fig. 1:

(1) input layer with n neurons;
(2) WTA output layer with m neurons.

The input layer consists of n neurons which provides matching scores MS_1, MS_2,…,MS_m from the input vector $\mathbf{x}^{\rightarrow}$ to each one of the exemplar vectors $\mathbf{e}_1^{\rightarrow}, \mathbf{e}_2^{\rightarrow}, \ldots, \mathbf{e}_m^{\rightarrow}$ which are stored in the weights of this layer [24]. The matching score is the number of matching elements between the input vector and the corresponding exemplar vector.

Considering a input vector $\mathbf{x}^{\rightarrow}=(x_1, x_2, \ldots, x_n)$ and an exemplar vector $\mathbf{e}_i^{\rightarrow}=(e_i^1, e_i^2, \ldots, e_i^n)$, where $i=1,\ldots,m$, the matching score (MS) is obtained from [13]:

$$MS_i = n - HD_i \qquad MS_i = n - \int_{j=1}^{n} |x_j - e_i^j| \tag{1}$$

where HD_i is the Hamming distance [13]. The Hamming distance is the number of elements in the input vector that do not match the corresponding exemplar vector.

These matching scores values are inputs for the WTA layer that determines which exemplar is closest to the given input vector $\mathbf{x}^{\rightarrow}$ [13].

3. SET Hamming network implementation

The first complete implementation at circuit level using tunnel junctions of a Hamming network is illustrated in Fig. 2.

The input layer in Fig. 2 is presented for the first time in this work. In this circuit, the input vector $\mathbf{x}^{\rightarrow}=(x_1, \ldots, x_n)$ is represented using input voltages. The synaptic weights are represented using capacitors C_{11}, C_{21}, C_{31},…,C_{1m}, C_{2m}, C_{nm}. In this way, input voltages injected in weight capacitances will result in pondered charges q_1, q_2,…,q_m expressed in Eq. (2).

$$\begin{aligned} q_1 &= x_1C_{11} + x_2C_{21} + \cdots + x_nC_{n1} \\ q_2 &= x_1C_{12} + x_2C_{22} + \cdots + x_nC_{n2} \\ &\vdots \\ q_m &= x_1C_{1m} + x_2C_{2m} + \cdots + x_nC_{nm} \end{aligned} \tag{2}$$

These charges will result in voltages $V_{\Sigma 1}$, $V_{\Sigma 2}$,…,$V_{\Sigma m}$ respectively at nodes Σ_1, Σ_2,…,Σ_m shown in Fig. 2.

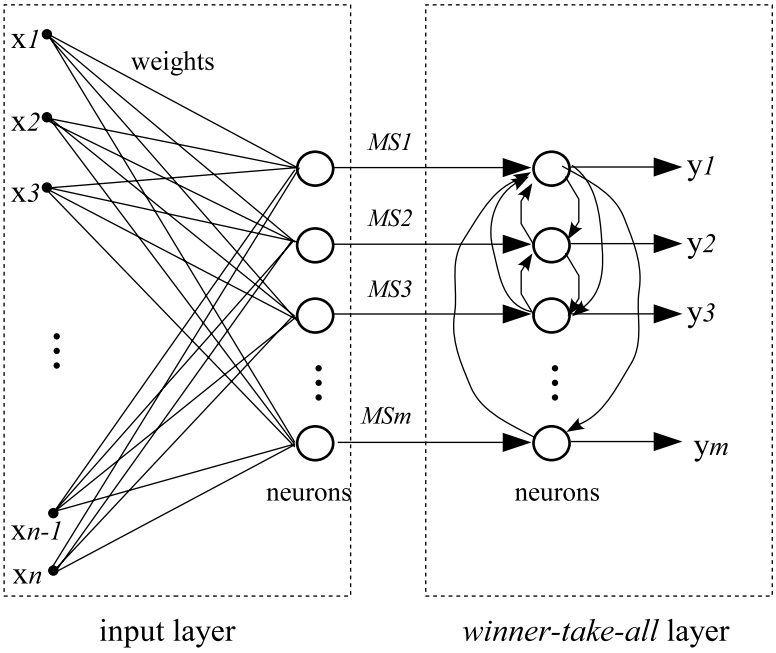

Fig. 1. Hamming network diagram.