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Leakage current study and relevant defect localization in integrated circuit failure analysis

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ABSTRACT

The purpose of integrated circuit (IC) failure analysis (FA) is to find and to explain failure root cause and mechanism, which helps IC designer and manufacturer to improve design and process. Leakage current presence within circuit is the main failure root cause among the FA cases, although the leakage currents within different circuits can stimulate a variety of IC failure modes. It is significant to study the leakage currents within ICs and to localize relevant defects quickly and accurately by the combination of some complementary FA techniques. However, it is difficult to identify the original leakage current from the consequential leakage currents and to locate the relevant defect.

In this paper, we explain the shape and location of a photon emission spot induced by an original leakage current is different from the one induced by a consequential leakage current. In a general case, and not only in this photon emission spot case, a method is elaborated to identify the original leakage current from the consequential leakage currents and to exactly locate the relevant defect by the combination of some complementary FA techniques. Some other functional failure cases will be studied to demonstrate adaptation and interest of this general method.

1. Introduction

Leakage current presence within IC is the main root cause among all the IC failure analysis (FA) cases, although the leakage currents within different circuits can trigger a variety of IC failure modes. This dramatically degrades IC reliability. FA is an effective method to study the leakage currents within ICs and to localize relevant defects. The failure mechanism revealed by FA is very important for improving IC reliability.

There are a lot of reasons or failure mechanisms that may result in leakage currents within ICs, such as electrical overstress (EOS), electrostatic discharge (ESD), implant defect, gate oxide rupture defect, metal bridge defect, p–n junction damage, latch up and so on. As semiconductor technology continues to move forward to smaller dimensions and to more complex circuit designs (thinner gate oxide layer and more metal layers), gate oxide rupture defect (fitting with silicon based defect) and metal bridge defect (metal based defect) have become two main and typical reasons inducing a leakage current within ICs. Generally, these two types of defects lead to complicated functional failures on ICs, so the leakage current study and defect localization are difficult and time consuming for FA engineers. Furthermore, they generate the leakage currents not only in the defect sites but also in other circuits linked to these defects. So the original leakage current stimulated by the defect conceals itself within the consequential leakage currents. It is a challenge for a FA engineer to identify the original leakage current generated by the defect from the consequential leakage currents and to precisely localize the relevant defect. It is difficult to do that only by one FA technique: some complementary FA techniques are needed and combined together.

Photon Emission Microscopy (PEM) [1–3] and Lock-in Infrared Optical Beam Induced Resistance Change (IR-OBIRCH) [4–6] are two effective FA techniques to analyze the leakage currents and to localize the relevant defects within ICs. They are non-destructive FA methods and can be performed both on topside ICs or backside ICs. Generally, PEM is employed in functional failure cases and Lock-in IR-OBIRCH is applied when a leakage current within an IC has been observed. Layout study is an effective method to analysis PEM and Lock-in IR-OBIRCH results. In Ref. [3], Hartmann has proposed a method combining PEM, OBIRCH and layout study to localize the metal bridge defects. However, sometimes the

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combination of PEM, OBIRCH and layout study does not offer a guarantee to identify the original leakage current from the consequential leakage currents and to localize the relevant defect. A microprobe analysis is often needed to confirm the result of that combination of PEM, OBIRCH and layout study. In this paper, a general methodology will be proposed to study the leakage currents using the combination of PEM, Lock-in IR-OBIRCH, layout study and microprobe analysis This method will be used for leakage currents induced not only by metal bridge defects but also by gate oxide rupture defects. The shape and location of a photon emission spot induced by an original leakage current or a consequential leakage current will be studied for identifying the original leakage current stimulated by the defect from the consequential leakage current. Some functional failure cases will be studied to demonstrate how to analyze the leakage currents within ICs and to localize relevant defects quickly and precisely by this method.

2. Methodology

A photon (light) emission is generated in active silicon semiconductor material according to two main mechanisms: field accelerated carriers and electron–hole recombination. The first mechanism is mainly observed in reverse-biased junction (i.e. Zener diode), MOS saturated transistor, ESD protection breakdown, gate oxide rupture defects and metal bridge defects. The second mechanism is predominant in forward biased junction and bipolar transistor in saturated mode [7]. Generally, MOS transistors in ICs work in on/off switch modes, and there is not current in CMOS (NMOS and PMOS) circuits under these two modes. Therefore, they do not emit photons (lights) under these two modes. A leakage in the active silicon semiconductor material does not fit with an on/off switch mode (since an on/off switch mode does not emit light) but this leakage fits with a stable mode (since a stable mode emits light). PEM technique employs a sensor to detect the photons emitted from active silicon semiconductor material. In this paper, a cooled Si-CCD sensor is employed in the PEM system and its detectable spectrum wavelength is about from 400 nm to 1100 nm. Photon emissions generated by both kinds of mechanisms emitting light, field accelerated carriers and electron–hole recombination, are detectable by the cooled Si-CCD sensor, but with a limited sensitivity. That is the reason why other FA techniques are needed.

Gate oxide rupture defect and metal bridge defect emit lights while they are being stimulated by electrical stress. Both of them generate also an intermediate voltage level in the linked MOS transistors, which makes these MOS transistors to work under a saturated mode. So, by these two types of defects, light is generated by the defects themselves but also by the linked MOS transistors put in a saturated work mode. The photon emission from saturated MOS transistors can be detected easily by PEM, because there are a lot of hot carriers in a saturated MOS transistor. However, photon emission detectability from these two types of defects by PEM depends on defect natures and on their leakage current and voltage drop level. Thus, sometimes both the original leakage current and the consequential leakage currents could be localized by PEM, but sometimes only the consequential leakage currents could be localized by PEM.

So, how to study these leakage currents after PEM analysis to identify the original leakage current stimulated by the defect from the consequential leakage currents and to localize the defect exactly? The answer is a layout study is firstly needed to identify where these leakage currents are on the layout. Different leakage current sources induce different photon emission spots on the layout, and the differences mainly refer to the different locations and different shapes of the photon emission spots on the layout. The following case studies will show the locations and shapes of the photon emission spots generated by three types of leakage currents (leakage current in a saturated MOS transistor, leakage current in the gate oxide rupture defect and leakage current in the metal bridge defect) are different. Thus, each kind of leakage current will be identified according to the location and shape of the photon emission spot during layout study.

If these two types of defects emit enough light that may be detected by PEM and if their locations and shapes are clearly identified on the layout, the original leakage currents generated by these defects can be identified easily and these defects can be precisely localized. Microprobe and Lock-in IR-OBIRCH analysis that typically follows the identification are not mandatory in this case. However, on the other hand, sometimes the photon emission generated by these two types of defects is not detected by PEM due to a limited PEM detector sensitivity, the defect nature or a too low electrical stress that crosses them. In this case, the photon emission spots generated by the consequential leakage currents has to be studied, which can provide some helpful clues to locate the original leakage current, and then infer where the original leakage current is on the layout: then, a microprobe analysis will be performed to confirm the conjecture. This process has to be repeated (study layout, proposing a hypothesis, performing microprobe) to narrow down the hypothesis and to finally find the original leakage current. In this case microprobe is definitely mandatory.

When the original leakage current has been revealed by microprobe analysis, Lock-in IR-OBIRCH should be used to precisely localize the original leakage current and relevant defect. IR-OBIRCH implements a 1340 nm laser to heat the die pixel by pixel while a constant DC voltage is being forced between two signals of the IC. Laser heat changes the characteristic of the defects or semiconductor devices while an OBIRCH spot is being marked on the die image synchronously. Lock-in mode of IR-OBIRCH can filter noise and improve signal to noise ratio (SNR). It can detect a minimum 10 pA current variation. Therefore, it is more effective to locate some smaller leakage currents compared to PEM, when the original leakage current has been caught by microprobe.

3. Cases study

3.1. Case study 1

This functional failure case involved an analog and mixed-signal IC. This IC has 8-output high side/low side switches with 16-bit serial input control. The functional failure mode was confirmed in the FA Lab: the output voltage of all 8 outputs on the failed IC was about 8 V instead of 12 V under 12 V power supply when they were switched on by 16-bit serial input control command under high side mode.

As this was a functional failure case, PEM was performed firstly under a functional set up to try to locate the defect. Two abnormal photon emission spots were localized on the failed IC compared with a reference part which revealed there were two leakage currents at the abnormal photon emission spots area. Fig. 1 shows the images about the abnormal photon emission spots on the failed IC. For identifying the original leakage current stimulated by the defect from the consequential leakage current and localizing the relevant defect, layout study was performed to examine these two abnormal photon emission spots. We found the abnormal photon emission spot 2 was much brighter than the abnormal photon emission spot 1 according to 200 magnification images. However, their locations and shapes could not be identified clearly only by 200 magnification images, so we had to zoom in these two abnormal photon emission spots area and 1000 magnification images were gotten in Fig. 1. Thus, locations and shapes could be clearly identified from 1000 magnification images. They were overlaid