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Vacuum effect on the void formation of the molded underfill process in flip chip packaging

Xue-Ru Guo, Wen-Bin Young *

Department of Aeronautics and Astronautics, National Cheng Kung University, Tainan 70101, Taiwan, ROC

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ABSTRACT

The flip chip packaging technology uses solder bumps for the electrical connection between the chip and substrate. A two-step procedure is usually used for the flip chip packaging. In the process, underfill material is filled into the gap between the chip and substrate by the capillary force. After that, epoxy molding compound (EMC) is used to overmold the entire assembly in a mold cavity through the process of the transfer molding. On the other hand, the molded underfill (MUF) process performs the packaging at a single step. In the MUF process, the EMC material fills the mold cavity with preplaced flip chip assembly, and finishes the underfill and overmold at the same time. In this study, experiments were performed to study the mechanism of the void formation in MUF. The effect of vacuum on the void formation was investigated. It was found that high quality of vacuum was necessary in order to eliminate the air pocket enclosed during the filling process. For different materials, the required vacuum quality may be different and it is well below the perfect vacuum.

1. Introduction

As more and more functions were integrated into a single integrated circuit chip, the I/O ports of a chip would also increase dramatically. The flip chip technology employed a surface for the electrical connection, where solder bumps attached on the chip surface were used to connect the chip and substrate directly. Since the coefficient of thermal expansion (CTE) of the chip and substrate are quite different, possible failures may occur as subjected to thermal load while in service. One way to resolve the problem of CTEs mismatch is to fill the gap between the chip and substrate with epoxy molding compound (EMC) and those EMC will encompass all the solder bumps. The flip chip packaging included two steps. One is the underfill process to compensate the CTEs mismatch and the other is to overmold the entire assembly [1–4].

The molded underfill (MUF) process combined the two steps in the original flip chip packaging into one single molding step and achieved both underfill and overmold at the same time. In the MUF process, multiple chips were mounted on a single large substrate and that was loaded into a mold cavity to fill in the EMC under an external pressure. When the heated EMC was injected into the mold cavity under pressure, it would flow into the gap between the chip and substrate and also the entire assembly simultaneously [3,5,6]. Khor et al. [7] studied the effect of solder arrangement on the MUF filling process. They also reported several studies on the fluid structure interaction during the MUF process [8,9].

Although, MUF has the advantages of fast and simple, it also creates other problems as flow unbalance and air pocket enclosure during the filling process. In the MUF, there are several different flow paths for EMC to fill in, including gaps between the chip and substrate, the chip and mold wall, and chip lines. Fig. 1 shows the cross section view of flip chips mounted on a substrate as assembled in the mold cavity. Since the three gaps have different sizes and flow resistances, it will result in flow unbalance during the mold filling process. The consequence of flow unbalance is the formation of air pockets at the downstream of the molding flow. If the air pocket cannot be eliminated in the process, it will result in voids after the packaging.

In order to eliminate the possibility of void formation resulted from the enclosed air pocket, vacuum might be applied to the mold cavity before the filing process. However, design of the molding process including the geometric and material parameters is necessary to reduce the problem of air pocket during the EMC filling. It was reported that a process simulation could be performed to investigate the effect of molding parameters on the filling patterns [7,10]. Commercial package could also be used for the 3D MUF process simulation [11]. Ong et al. [12] studied the microbump pitch effect in MUF by a numerical model. They found that small bump

* Corresponding author.
E-mail address: youngwb@mail.ncku.edu.tw (W.-B. Young).

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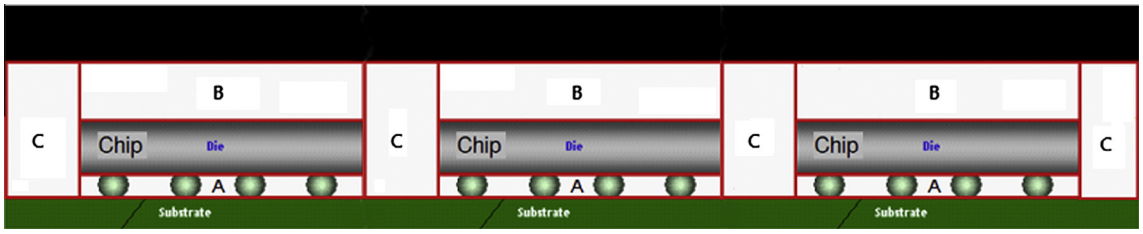

Fig. 1. Schematic diagram of the cross section of the molded underfill cavity.

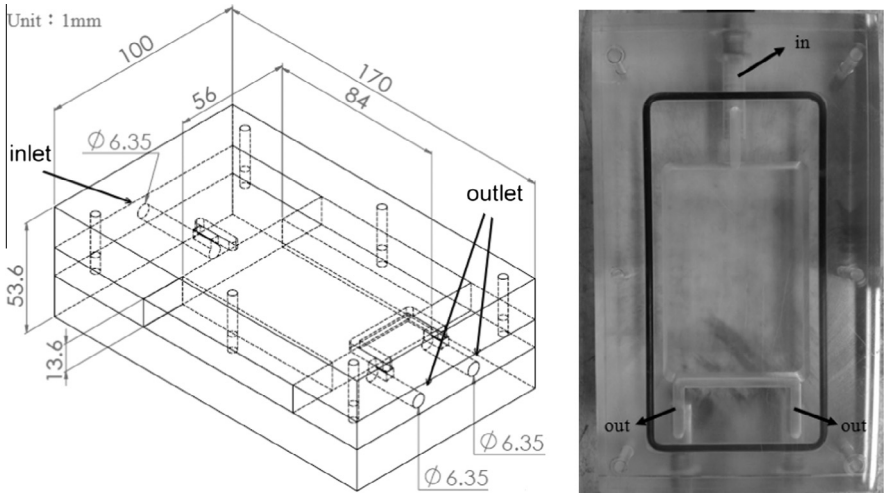

Fig. 2. Design of the transparent transfer mold and the top view of the mold where one inlet from one side and two outlets at the other side.

pitch may have more chance to trap air pockets behind the bumps. Those simulation models were demonstrated to be effective tools to reduce the design-to-implementation cycle time.

Since the void formation problem was difficult to be avoided with the design of geometric parameters in MUF, vacuum applied in cavity was necessary to eliminate the void formation. Theoretically, there will be no void forms in the cavity if the vacuum quality is high enough to expel all the air. In the packaging process, small voids may still exist below the chip due to the low vacuum quality.

2. Experimental

A transparent mold made of acrylic plates was constructed for the visualization of the void formation during the MUF process. Two thick acrylic plates were bolted together with sealing o-ring located at the interface. One of the plates was cut a rectangular region to form the cavity. The designed mold cavity is $84 \times 56 \times 13.6\ mm^3$ as shown in Fig. 2. One inlet was located at the center of one end and two outlets were designed at the two corners of the other end. The dimension of the substrate is $84 \times 56 \times 10\ mm^3$ and the chip is $20 \times 20 \times 1\ mm^3$. Three chips were attached to the substrate by adhesives with four solder bumps located at the corners of the chip. The solder bump has a diameter of 600 μm. The resulted cavity will have a height of 0.6 mm for region A, 3 mm for region B, and 13.6 mm for region C. The three regions were shown in Fig. 1.

The transparent mold was used to investigate the flow unbalance in the MUF process. Usually, the chips are attached to the substrate with regular array. If a line gate was used for the transfer molding, the flow field along a line of chip will be symmetric as shown in Fig. 3. Therefore, only one line of chips was used to study the flow field. As shown in Fig. 1, there are three flow paths for the

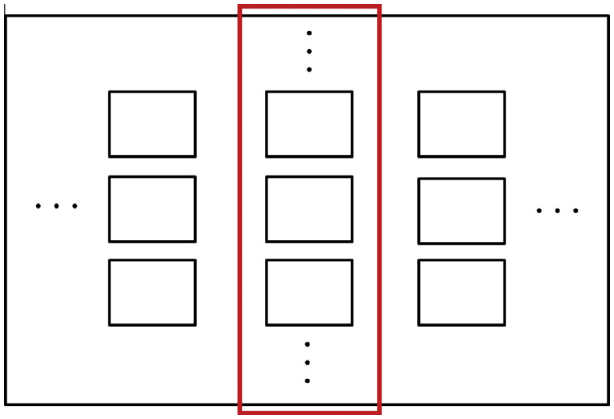

Fig. 3. Design of the chip layout on the substrate for flow visualization.

EMC to flow over the entire cavity. Each flow path can be considered as a rectangular channel. The flow unbalance is because of the different flow resistances induced by the different heights of those channels. In this study, only four solder bumps were used to attach the chip so that they have nearly no effect on the flow field. The solder bumps were located near the four corners of the chip with a distance of 2 mm to the edges. If a full array of solder bumps was considered, it would increase the flow unbalance due to the increase flow resistance of the flow path under the chip.

For a vacuum assisted MUF process, the inlet port was closed at the beginning and vacuum was applied from the outlet ports for several seconds. Depending on the cavity size, the time to reach the maximum vacuum quality by a specific vacuum pump may be different. A vacuum pump UC-OLD-10 from Uni-Crown, Taiwan,