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A comparison of heavy ion induced single event upset susceptibility in unhardened 6T/SRAM and hardened ADE/SRAM

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ABSTRACT

Single event upset (SEU) susceptibility of unhardened 6T/SRAM and hardened active delay element (ADE)/SRAM, fabricated with 0.35 μm silicon-on-insulator (SOI) CMOS technology, was investigated at heavy ion accelerator. The mechanisms were revealed by the laser irradiation and resistor-capacitor hardened techniques. Compared with conventional 6T/SRAM, the hardened ADE/SRAM exhibited higher tolerance to heavy ion irradiation, with an increase of about 80% in the LET threshold and a decrease of ~64% in the limiting upset cross-section. Moreover, different probabilities between 0 → 1 and 1 → 0 transitions were observed, which were attributed to the specific architecture of ADE/SRAM memory cell. Consequently, the radiation-hardened technology can be an attractive alternative to the SEU tolerance of the device-level.

1. Introduction

For the conventional six transistors (6T) SRAMs, the radiation response to single events exhibited an increased susceptibility that has been produced from lower operating voltage, higher speeds and decreasing feature sizes. These characteristics conspired to result in a significant reduction of single event upset (SEU) critical charge [1]. On the other hand, technological advances of science, especially silicon-on-insulator (SOI) technology, had a deep influence on radiation hardened applications in the integrated circuit (IC) field over the past 50 years [2,3]. Hardened techniques against single event effects (SEEs) are mainly divided into three categories: the device-level, circuit-level and system-level [4]. These techniques have built a bridge between the physical mechanisms and the IC-level analysis and applications. In the hardened device-level, the typical approach to SEU mitigation within the conventional 6T/SRAM cell is to couple the invertors with passive delay elements such as the resistors, capacitors, as well as diodes or their combinations [5–9]. However, this approach costs the extra write-time to decrease the SEU susceptibility. To minimize the extra write-time, an active delay element (ADE) was applied to harden the 6T/SRAM cell in this work. Essentially, the ADE is an NMOS transistor fabricated in partially depleted SOI technology. For convenience, in the subsequent sections, 6T/SRAM and ADE/SRAM refer to the conventional 6T SRAM and ADE SRAM, respectively.

In previous research, a double-hit (DH) mechanism was proposed to explain the limiting proton upset cross-section of such SOI SRAM [10]. Moreover, the DH mechanism has been developed and successfully applied to explain the experimental results of ADE/SRAMs induced by proton and heavy ion irradiation [11,12]. Liu et al. reported that the limiting upset cross-section of a full transmission (FT)-ADE SRAM cell was nearly three orders of magnitude smaller than the sum of the vulnerable gate areas [12]. However, in our work, the limiting upset cross-section is of the same order of magnitude with that of the ADE/SRAM. In other words, the DH mechanism cannot explain the obtained results. In this work, the resistor-capacitor (RC) delay mechanism was applied to explain the results appropriately, and different probabilities of 0 → 1 and 1 → 0 transitions have been found with reasonable interpretations. Moreover, to verify the assumption, the laser test was performed accurately.

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2. Experimental details

2.1. Devices under test (DUT)

The DUTs used in the experiments were fabricated with 0.35 μm SOI CMOS technology by the Institute of Microelectronics, Chinese Academy of Sciences (IMECAS). The supply voltage of DUTs was maintained at 5 V and the capacity was 64 Kbit with the dual in-line package (DIP). The thickness of the buried oxide and silicon film were 150 nm and 260 nm, respectively. The schematics of 6T/SRAM cell and ADE/SRAM cell are shown in Fig. 1. When the switch of ADE is closed (i.e. WL = V_{dd}), the value of ADE resistance is sufficiently low so that it cannot affect the write speed, while the switch of ADE is opened (i.e. WL = 0), the high ADE resistance considerably improves the SEU tolerance. Note that the ADE resistance is equal to zero, the ADE/SRAM cell turns to the 6T/SRAM cell.

2.2. Experiment setup

The heavy ion experiments were carried out at the Heavy Ion Research Facility in Lanzhou (HIRFL) cyclotrons in Institute of Modern Physics, Chinese Academy of Sciences (IMPCAS). Two kinds of heavy ions (i.e. ^{86}Kr and ^{209}Bi) were used for the irradiation of the DUTs, with initial energies of 25 MeV/u and 9.5 MeV/u, respectively. All the experiments were carried out in air at room temperature with the normal incidence except for the case where the effective LET was 52.6 MeV cm^2/mg ($\theta = 50°$) and 68.0 MeV cm^2/mg ($\theta = 60°$). The higher effective LET was acquired by adjusting the angle of ion incidence (θ), according to the relation LET(θ) = LET(0)/cos(θ). In the experiments, along ion beam direction, the heavy ions first penetrated through certain thickness of plastic scintillator (BC408) for monitoring the number of the ions and then a Ti-window for vacuum sealing. In the next step, using different thicknesses of Al-foils degraders and/or the air, the desired energy was adjusted for a specific experiment. For ^{86}Kr and ^{209}Bi ions, the thickness of BC408 was 21 μm and 12.5 μm and the Ti-window was 24.7 μm and 14.7 μm, respectively. Details of the experimental parameters are shown in Table 1. The LET and range of the ions in silicon were calculated by using SRIM2013 code [13,14].

All the DUTs were decapped before the irradiation process and the tests were carried out in a dynamic mode. Before the irradiation, a checkerboard pattern was written into the DUTs through a field programmable gate array (FPGA)-based tester. After that, the FPGA began to scan the data in the DUTs. Until one error was detected, the error address, the error bit and the error time were recorded in a document. In order to ensure the proper function of the DUTs, the current of DUTs was monitored carefully. The flux of irradiation was adjusted in such a way that one error appeared per second. With reliable statistics, each test ended with the number of errors reaching to 200. The SEU cross-section (σ) with the unit of cm^2/bit was calculated by the following equation.

$$\sigma(\mathrm{cm}^2/bit) = \frac{N_{upset} \cdot A}{F \cdot C \cdot cos\theta} \quad (1)$$

Where N_{upset} is the number of upset errors, A refers to the area of the beam spot with the unit of cm^2, F is the number of total incident ions, C denotes the capacity of the DUT with the unit of bit and θ indicates the angle of incidence.

3. Results

3.1. Comparison of SEU susceptibility in ADE/SRAM and 6T/SRAM

Experimental results of our measurements are shown in Fig. 2, which are fitted by using Weibull function. Weibull function is widely used to fit the direct ionization (heavy-ion) SEU cross-section data. This function provides great flexibility in fitting the LET threshold in the cross-section and naturally levels to a plateau or limiting upset cross-section [15]. The relation for the Weibull function is given below.

$$\sigma = \begin{cases} \sigma_{sat}\left[1 - \exp\left\{-\left(\frac{LET - LET_{th}}{w}\right)^s\right\}\right] & LET \geqslant LET_{th} \\ 0 & LET < LET_{th} \end{cases} \quad (2)$$

Where LET is Linear Energy Transfer in MeV·cm^2/mg, σ refers to the SEU cross-section in terms of cm^2/bit, σ_{sat} is the limiting or plateau upset cross-section with unit of cm^2/bit, LET threshold (LET_{th}) is the minimum LET to observe a flip of the stored value, w is the width parameter, and s is a dimensionless exponent.

LET_{th} and σ_{sat} are the most important parameters to characterize the SEU sensitivity of a device. As can be seen in Fig. 2, for 6T/SRAM cell, LET_{th} is 15.7 MeV·cm^2/mg and σ_{sat} is 4.4×10^{-8} cm^2/bit that is larger than the gate area of an off-NMOS transistor ($\approx 6.8 \times 10^{-9}$ cm^2/bit) or an off-PMOS transistor ($\approx 4.5 \times 10^{-9}$ cm^2/bit). This indicates that the sensitive area may be extended into the drain and/or the body-tie region [16]. For ADE/SRAM cell, LET_{th} is 28.3 MeV·cm^2/mg and σ_{sat} is 1.6×10^{-8} cm^2/bit which is also larger than the gate area of an off-NMOS transistor or an off-PMOS transistor. Note that, for the DH mechanism, the limiting upset cross-section is three orders of magnitude smaller than the gate area of a transistor [12]. However, the limiting upset cross-section of ADE/SRAM is larger than the gate area that

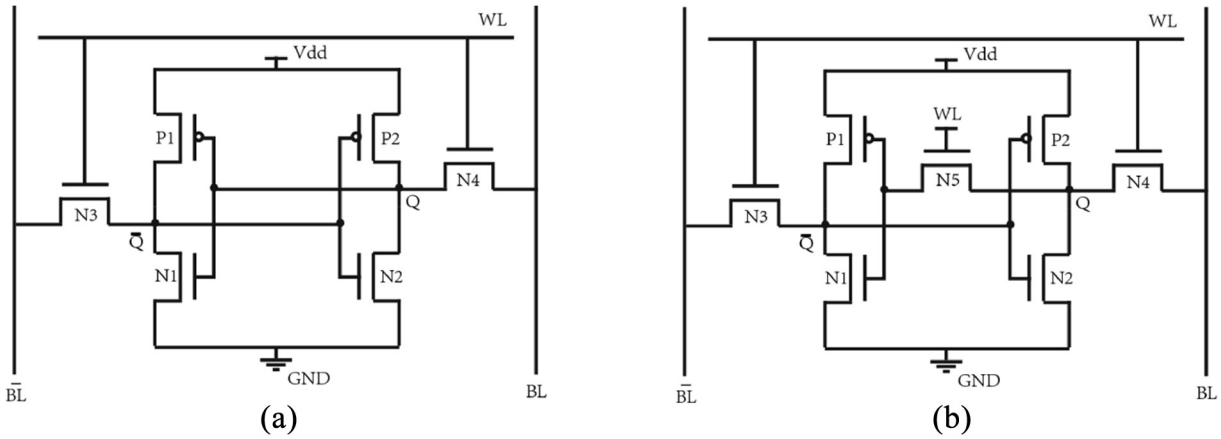

Fig. 1. Schematics of the two memory cells (a) conventional 6T/SRAM (b) ADE/SRAM.

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