Microelectronics Reliability 55 (2015) 645–653

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Cross-layer investigation of continuous-time sigma–delta modulator under aging effects

Hao Cai *, You Wang, Kaikai Liu, Lirida Alves de Barros Naviner, Hervé Petit, Jean-François Naviner

Département Communications et Electronique, Institut Mines-Télécom, Télécom-ParisTech, LTCI-CNRS-UMR 5141, Paris CEDEX 13 75634, France

ARTICLE INFO

Article history:
Received 14 August 2013
Received in revised form 19 November 2014
Accepted 20 November 2014
Available online 5 December 2014

Keywords:
Aging mechanisms
Cross-layer
Hierarchical analysis methodology
Failure analysis
Continuous-time (CT) sigma–delta (ΣΔ) modulator

ABSTRACT

In order to achieve reliability study in large and complex analog and mixed signal (AMS) circuits and systems, it is required to develop effective reliability-aware design methodologies and exploration tools. This paper discusses two aging mechanisms: hot carrier injection (HCI) and negative bias temperature instability (NBTI) and their effect on 65 nm CMOS integrated circuits and systems (ICs). We propose an aging-aware cross-layer approach to comprehensively evaluate aging induced performance degradation at the abstraction (system) level. This approach is composed by hierarchical aging analysis at transistor/circuit level, block failure analysis at abstraction level and system-level aging considerations, which can essentially highlight sensitive blocks for circuit designers. This approach is demonstrated with a continuous-time (CT) sigma–delta (ΣΔ) modulator. Analog loop filter and clock distributor are studied with failure boundary and transistor level aging simulation. The aging investigation approach reports system level aging-aware consideration of these building blocks. Results show that amplifiers in analog loop filter have enough margin to cope with aging induced degradations. However, aging risk exists in clock circuits, especially when implementing with high V_t transistors. NBTI induced clock jitter from clock distributor can influence clocked block in CT ΣΔ modulator and degrade signal-to-noise ratio (SNR).

1. Introduction

Reliability issues become important in integrated circuits and systems [1]. Temporal aging effects such as hot carrier injection (HCI) and negative bias temperature instability (NBTI) can cause performance degradation during circuit lifetime [1]. In order to estimate aging induced degradations and predict ICs usage time, reliability-aware (or aging-aware) methodologies have been proposed in recent years [2].

Continuous-time (CT) sigma–delta (ΣΔ) modulators are popular in analog-to-digital converters (ADC) due to inherent anti-aliasing filtering and low power consumption [3]. However, it is less robust against jitter effects and excess loop delay compared with their discrete-time (DT) counterparts [4]. All clocked components (e.g., switches, quantizer and digital-to-analog converter (DAC)) are sensitive to clock uncertainty [5]. On the other hand, nonidealities in analog loop filter, e.g., finite operation amplifier (op-amp) DC gain and bandwidth can impact modulator performance [6]. Due to the continuously scaling down of CMOS technology, aging problems can further degrade these nonidealities parameters in CT ΣΔ modulators.

Clock unit is an essential block in CT ΣΔ modulator. Unreliable clock unit can in fact cause clock uncertainty (either deterministic skew or stochastic jitter [7,8]). Both skew and jitter are the time-deviation of the clock transitions with respect to the ideal clock [9]. Skew is always a fixed constant from cycle to cycle, whereas jitter is typically subject to normal distribution and it can change quickly from cycle-to-cycle or slowly over many clock cycles. Jitter is always harmful but sometimes skew could be beneficial [8].

For large and complex analog and mixed signal (AMS) circuits and systems, efficient reliability predictions rely on proper analysis methodologies. In this paper, hierarchical reliability analysis and block failure estimation are used. Based on these methods, an aging-aware approach is proposed to estimate aging mechanisms at the abstraction (system) level. A 3-bit low-pass (LP) third-order CT ΣΔ modulator is applied to demonstrate this approach. Aging aware considerations are directed towards building blocks of CT ΣΔ modulator.

The paper is organized as follows: Section 2 reviews HCI and NBTI aging mechanisms in MOS transistors. Section 3 presents the hierarchical reliability analysis and block failure estimation at the abstraction level of complex AMS systems. The cross-layer aging investigation approach is proposed. In Section 4, we demon-

* Corresponding author. Tel.: +33 1 4581 7661; fax: +33 1 4580 4036.
E-mail address: cai@telecom-paristech.fr (H. Cai).

http://dx.doi.org/10.1016/j.microrel.2014.11.015
0026-2714/

strate this proposed approach with CT ΣΔ modulator. Aging-aware considerations are elaborated on analog loop filter and clock distributor, which designed with 65 nm CMOS technology. Finally, conclusions are posed in Section 5.

2. Problem statement

Aging mechanisms occur at physical level of CMOS transistors. Based on simulation tools, designers can realize aging induced degradation at transistor and circuit levels.

2.1. Aging effects

2.1.1. Negative bias temperature instability

NBTI becomes a dominant reliability issue for sub-micron PMOS transistors [10,11]. When negative gate bias is applied to PMOS, transverse electric field is formed across gate oxide. The generation of interface traps at the Si–SiO_2 can cause threshold voltage (V_T) increase. Predictive modeling of NBTI effect with reaction–diffusion (R–D) mechanism shows NBTI characteristics such as stress-recovery phase, temperature dependence and frequency independence [11]. In clock circuits, Chacraborty et al. highlighted NBTI induced clock skew can increase by up-to 7× in gating enabled clock trees [12]. Recently, a new viewpoint of stochastic NBTI has been proposed in [13], inverters under NBTI can generate aging-independent jitter due to random telegraph noise (RTN).

Li et al. [14] proposes a NBTI accelerated-lifetime model (see Table 1), the lifetime t_f is defined as the time to a fixed degraded V_{th} value. A_{NBTI} is the process related prefactor, V_{gs} and T is gate-source voltage and temperature. k is Boltzmann's constant, α denotes the voltage acceleration factor, E_a is the activation energy. Table 1 presents threshold voltage shift model of NBTI, where E_{ox} is oxide electric field, C_{HC}, α_1 and α_2 are technology-dependent parameters [15].

2.1.2. Hot carrier injection

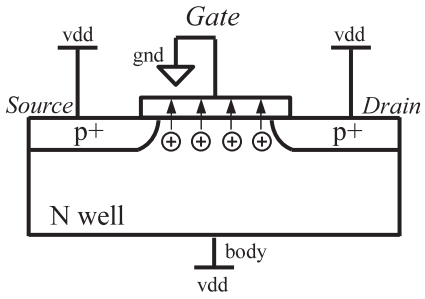
Hot carrier injection emerges from the shrinking of transistor dimension and the electric field increasing in the channel. It is a temporal aging unreliability effect as the density of interface states (N_{it}) produced by channel carriers peaks near the drain edge of the gate. When NMOS transistor switches on, hot electrons can overcome the potential barrier and inject into gate oxide due to high lateral electric field near the drain and Fig. 1(b). It causes the generation of the interface traps at the Si–SiO_2 interface which result in transistor parameters shift over time, e.g., V_T increase and the electron mobility (μ).

There is no recovery phase in HCI since the annealing involving passivating a broken Si–H bonds towards a point of broken Si–H bonds [11]. CMOS Technology scaling causes voltage reduction, the relative lower drain current I_d will reduce HCI effects. However, this is not always feasible for gate lengths less than 50 nm. There is no significant reduction in gate voltage which is planned for additional scaling.

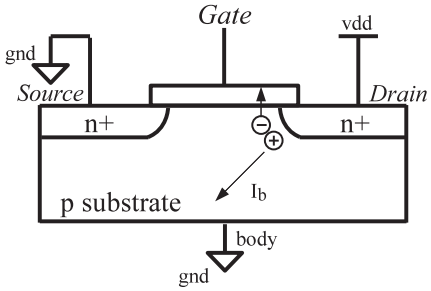
Li et al. [14] also proposes the HCI lifetime model (see Table 1), where E_{aHCI} is the apparent activation energy, n is a technology dependent constant, and A_{HCI} is the model prefactor.

Table 1
NBTI and HCI prediction models: time to failure and threshold voltage shift [14,15].

	Time to failure (t_f)	Threshold voltage shift (ΔV_{th})
NBTI	$A_{NBTI} \cdot \left(\frac{1}{V_{gs}}\right)^{\alpha} \cdot \exp\left(\frac{E_a}{kT}\right)$	$C_{HC}\frac{1}{\sqrt{L}}\exp(\alpha_1 E_{ox})\exp(\alpha_2 V_{DS})t^{n_{HC}}$
HCI	$A_{HCI} \cdot \left(\frac{I_{sub}}{W}\right)^{-n} \cdot \exp\left(\frac{E_{aHCI}}{kT}\right)$	$\exp(\alpha_3 E_{ox})\exp\left(\frac{-E_a}{kT}\right)t^{n_{BTI}}$



(a) NBTI causes positive oxide charge and interface traps in PMOS type transistors



(b) Hot carriers inject into the dielectric at the drain end of NMOS type transistors

Fig. 1. HCI and NBTI mechanisms at CMOS device level.

2.2. Low layer review of aging problems

Here, we investigate the transistor type *svtlp* (low power with standard V_T) in 65 nm CMOS technology, which is modeled with a BSIM4 parameters [16]. The transistor dimension is set to $W = 0.36$ μm, $L = 0.06$ μm, where L is minimum transistor length.

2.2.1. Physical level

At physical level, aging effects can degrade some BSIM4 parameters then influence transistor performance. The degradation of physical parameters are highly dependent on the transistor aging duration time.

As shown in Fig. 2(a), HCI can influence sub-threshold swing coefficient (n_{fac}), intrinsic threshold voltage (v_{th0}), intrinsic mobility (μ_0), saturation velocity (v_{sat}), drain source resistance per width (r_{dsw}), subthreshold region DIBL coefficient (eta_0) and threshold voltage offset (v_{off}). The correlation analysis is used to filter out some correlated parameter. v_{th0}, μ_0, n_{fac} and r_{dsw} are selected as the main degraded parameters of NMOS transistor. Besides, the only BSIM4 parameter affected by NBTI is v_{th0} of PMOS transistor (see Fig. 2(b)). More severe v_{th0} degradation is observed when PMOS transistor work at high temperature (150 °C).

We select one year aging time as an example point. As shown in Fig. 2(a) and (b), since from t_0 (fresh) to one year, the degradation is more severe than the later periods (e.g., aging degradation from one year to two years).

In Table 2, dominant BSIM4 parameters are sorted out as aging sensitive and non-sensitive. In NMOS transistor, the dominant aging nonsensitive BSIM4 parameters include: length variation (x_l), width variation (x_w), gate oxide thickness (t_{ox}) and channel doping concentration (n_{dep}). In PMOS transistor, except v_{th0}, other parameters mentioned above are aging non-sensitive.

2.2.2. Transistor/gate level

In low power transistor family, different V_t transistors can be used for performance tradeoff (e.g., leakage-power, delay and