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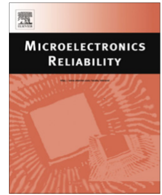

Accurate reliability analysis of concurrent checking circuits employing an efficient analytical method ☆

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ABSTRACT

Transient faults are important concerns in emerging ICs built from deep semiconductors. Concurrent error detection (CED) scheme has been proved to be an efficient technique in such a context. On the other hand, the increase of multiple faults can be foreseeable in future ICs. However, reported efforts applied to quantify the efficiency of CED schemes mostly consider single faults or suppose that implemented checker mechanisms are fault-free. This paper describes an alternative analytical solution for CED circuits analysis under a more realistic hypothesis. In addition to the assumption of the whole fault-prone circuit (including checker mechanisms), different failure rates of logic gate are considered as well. The proposed approach is based on probabilistic transfer matrices and then can deal with multiple faults. The time efficiency of the proposed solution is demonstrated through arithmetic circuits. By applying this solution, classical CED schemes are discussed according to different failure rates of transistor.

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1. Introduction

The steady decreasing of CMOS geometrical dimension is leading a reliability reduction of integrated circuits (ICs) [1]. Electronic devices became more susceptible to faults caused by temporary environmental conditions such as alpha and neutron particles [2], and thermal noise [3]. Radiation-related effects induced transient faults (i.e., soft errors) are one of the main error experiences suffered by ICs during usage phase [4]. These transient faults manifest themselves as random independent one time errors (e.g., temporal inversion of a bit value).

A transient fault in a logic block can propagate to primary outputs and be captured by the memory cells only if it is not filtered by any of the following making properties [5]:

- *Electrical masking* which occurs when a glitch fault is attenuated by subsequent logic gates due to the electrical properties (i.e., the glitch does not have enough duration or amplitude to propagate to outputs).
- *Temporal masking* which indicates that an error arrives at the output latch at the time of latching rather than the clock transition (where the input value of a latch is captured).
- *Logical masking* which appears when a fault occurs at non-sensitized path of a circuit.

Logic circuit is normally considered less susceptible to transient faults than memory elements for the masking properties [6]. However, the contribution of soft errors in logic circuit has been predicted to exceed the memory cells with the continuous downscaling of CMOS technology [7].

Fault tolerant approaches have been widely applied to cope with these faults. Among them, triple modular redundancy (TMR) is famous for reliability improvement. This scheme can mask all faults on a single module regardless of the faults correlation. Despite of the efficiency for fault masking, the classical TMR approach requires high hardware redundancy. *Concurrent error detection* (CED) techniques are well known for the detection of errors occurring during normal operation, thereby can efficiently cope with the soft errors on logic circuits. Various CED schemes have been presented in the last decades [8–11]. Whatever the approach is, the use of redundant resources in CED schemes implies the overhead. Attaining a good tradeoff between reliability and overhead is essential to an effective design [12].

Most often, the characterization of a CED scheme relies on single fault hypothesis [13,14]. However, multiple faults should be considered henceforth for deep-submicron CMOS ICs [15–17]. A single radiation particle struck may induce the faults on different nodes in the combinational circuit. Multiple faults analysis of CED schemes have been only reported in few literature and most

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of them assume that faults do not affect fault-check parts [18]. Vasconcelos et al. proposed a fault injection and functional simulation approach where every component in a circuit is fault-prone [19]. The authors concentrate on the logical masking ability of logic circuits, the most intractable masking property to be analyzed. The time complexity of this approach is exponential with the number of binary inputs and the number of gates in the circuit, which limits the number of injected faults and then the accuracy of the obtained results.

Analytical approaches have been demonstrated be helpful to cope with multiple faults [20–23]. But they focus on *signal probability* defined as the probability that all circuit outputs are correct and can not be directly applied to analyze CED circuits. Besides, aforementioned methods generally assume individual gates failures as a constant value. In fact, the radiation-related effects affect ICs on transistor level, particularly the negative-biased transistors. As a consequence, the gate failure probability changes with the input vector and the gate topology [24,25].

In this paper, we present a method suitable for reliability assessment of CED circuits with respect to logical masking property. The fundamental is *probabilistic transfer matrix* (PTM) which is an accurate analytical method [20]. We devote to *functional reliability* that takes into account the role of checkers. A gate structure-aware fault model for logic gate is applied to achieve a more realistic estimation. With the help of this method, we explore how multiple faults affect different CED circuits as well as the impact of transistor's sensibility.

The paper is organized as follows: Section 2 reviews some background of this work. Section 3 recalls CED basics and how this kind of circuit can be analyzed by fault injection. Section 4 presents simulation results, while Section 5 discusses classical CED schemes based on the proposed method. Finally, conclusions of this work are outlined in Section 6.

2. Preliminaries

2.1. Functional reliability of CED circuits

The general scheme of a Concurrent Error Detection (CED) structure is composed of three blocks: a target function F, a function predictor F_p (which predicts some special characteristics z of F's output y) and a function checker F_c (which checks if these characteristics are satisfied by F's output), as seen in Fig. 1. The checking of F_c results in a one-bit output e. In the remainder of this paper, it is assumed that $e = 0$ when no error is detected and $e = 1$ otherwise. This is solely a convention and does not mean a restriction. The analysis of such a CED shows that it can produce four exclusive events:

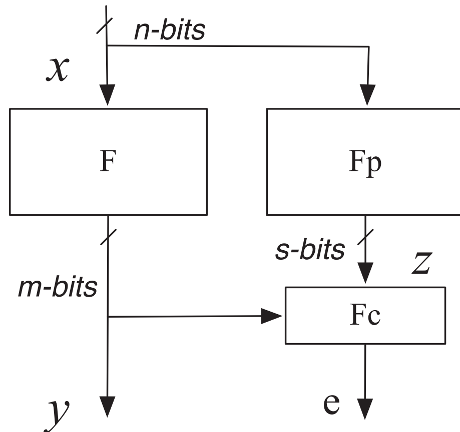

Fig. 1. Concurrent error detection circuit.

E_1: when the checker indicates a correct operation and the circuit output is correct.
E_2: when the checker indicates an incorrect operation and the circuit output is incorrect.
E_3: when the checker indicates an incorrect operation and the circuit output is correct.
E_4: when the checker indicates a correct operation and the circuit output is incorrect.

Functional reliability is defined as the ability of a system or component to perform its required functions under stated conditions for a specified period of time, even in presence of faults [26]. Therefore, we can state that functional reliability of a CED circuit is related to the probability of producing only the events E_1 or E_2. Consequently, the functional reliability is expressed as:

$$R_{CED} = p(E_1) + p(E_2) \tag{1}$$

2.2. CED analysis by fault injection

The principle of the approach described in [19] is to analyze the CED circuit under all possible fault configurations for each possible input vector. The framework shown in Fig. 2 is utilized to examine the above mentioned four events. As illustrated in Fig. 2, a fault free circuit works simultaneously as a reference for fault-prone CED circuit. The correctness of output is indicated by f_i in which the value "1" means a correct y, and vice versa. Each event is related to a combination of $\{e, f_i\}$. For example, E_3 is considered occurring when both f_i and e are "1".

The computation of each event's probability is based on *Probabilistic Binomial Reliability* (PBR) proposed in [27] as followed:

$$P(E_i) = \sum_{k=0}^{G} p(k) c_k(E_i), \quad i \in 1,2,3,4 \tag{2}$$

where G is the gate number of circuit, $p(k)$ denotes the probability of appearing k simultaneous faults and $c_k(E_i)$ represents the percentage of occurring event E_i considering all input combinations and k faults. The accuracy in this analysis is ensured by performing an exhaustive functional simulation and leads to a computational complexity exponential with the number of binary inputs and the number of gates in the circuit. Computational complexity optimization can be achieved by reducing the number of simultaneous faults considered. Consequently, in this case accuracy can not be ensured.

2.3. Probabilistic Transfer Matrices (PTM)

Consider a logic block b with n-bits input x and m-bits output y, where $x \in \{x_0, x_1, \ldots, x_i, \ldots, x_{2^n-1}\}$ and $y \in \{y_0, y_1, \ldots, y_j, \ldots, y_{2^m-1}\}$. Both of them have binary representations. For instance, "1111" represents x_{15} when n is "4". The PTM of block b, denoted PTM_b, has $2^n \times 2^m$ elements. In this matrix, each element in coordinate

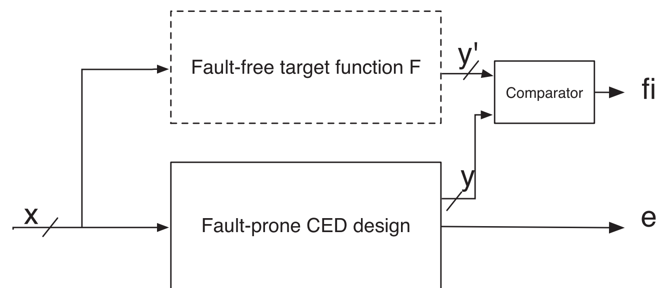

Fig. 2. Framework proposed in method [19].

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