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Electrical Overstress of Integrated Circuits

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ABSTRACT

Common misconceptions regarding electrical overstress (EOS) and the failure characteristics of integrated circuits (ICs) are summarized, analyzed and clarified. In order to avoid EOS fails right from the beginning of the IC design process, a methodology is proposed that accounts for the special characteristics of ICs and their applications in order to deal with EOS in the design, handling and application of ICs.

1. Introduction

There is a trend driven by system manufacturers to integrate more and more "EOS protection" on-chip due to cost, overall form factor and performance reasons [1]. Unfortunately, many users of ICs often do not distinguish between the different causes of EOS [2,3]. E.g. users expect the integrated component-level ESD (CL-ESD) protection of ICs not only to withstand any CL-ESD event but also to protect ICs from system-level ESD (SL-ESD) and other kinds of electrical stress. This lack of distinction has unintentionally been encouraged over many years by IC manufacturers, who classified field returns, which were caused by specific types of EOS, simply as "EOS/ESD" [3]. Moreover, despite the remarkable advances in ESD control, many users of ICs still cling to meanwhile out-dated ESD requirements, e.g. 2 kV human-body-model (HBM) [4], or misinterpreted models, e.g. the so-called "machine-model" (MM) [5]. At the same time, IC manufacturers are required to supply "EOS robust" ICs to their customers without knowing the final application and its electrical stress requirements [1].

These inconsistencies cause several replacement processes and result typically in a trial-and-error development process to design "EOS robust" ICs (cf. Fig. 1). Unfortunately, only a few electrical stress requirements (e.g. CL-ESD and latch-up (LU) requirements) are generally specified by system manufacturers (1). Other electrical stress requirements though needed are often neglected and are therefore shaded in grey in Fig. 1. Hence, IC manufacturers have to get by with the knowledge that they have learned from previous designs and analyses of competitor ICs (2) in order to design "robust" ICs (3). Since on the other hand system manufacturers are not aware of the failure characteristics of ICs and of the electrical stress they are exposed to in their manufacturing and application environments, system manufacturers often compare compatible ICs of competitors to select the most "robust" one (4). Unfortunately, this trial-and-error process causes often unpleasant surprises, e.g. when an IC with an excellent CL-ESD immunity fails for another kind of electrical stress. In this case, system manufacturers often request failure analysis reports and detailed information on the failing IC from the IC manufacturer (5). Unfortunately, they generally do not provide much information on the conditions that caused the failure. As a result, IC manufacturers typically run failure analyses in order to find the root cause of the failure and try to fix it by a re-design of the IC (6). If the root cause of the failure cannot be found and ICs still fail, some system manufacturers respond to the assumed lack of "EOS robustness" by increasing their CL-ESD and LU requirements or by asking for robustness validation of ICs (7). Finally, they rate IC manufacturers based on the "EOS robustness" of their ICs.

The aforementioned inconsistencies and the problems they cause are often due to common misconceptions regarding ICs and EOS. These misconceptions and the desire for simple EOS solutions are often encouraged by today's tight time-to-market and cost requirements [6]. Therefore, it is important to understand and accept that physics does not respond to time-to-market and

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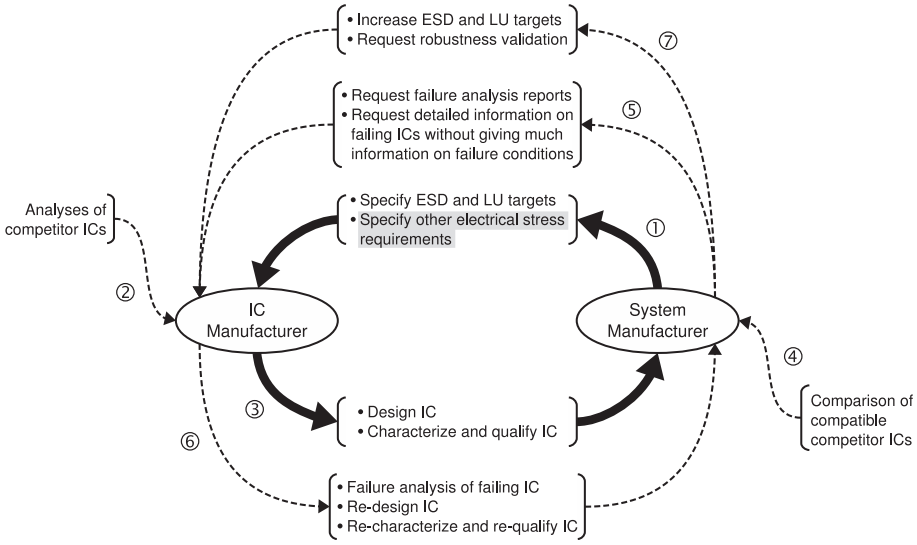

Fig. 1. Typical trial-and-error development process to design "EOS robust" ICs. (The chronological sequence is indicated by the digits 1–7).

cost requirements. Only by taking into account the characteristics of ICs, their application systems and the different kinds of electrical stress that they may experience, it is possible to protect them from EOS.

Given these facts, it is the purpose of this paper to clarify the failure characteristics of ICs, to present typical causes of EOS and to propose a methodology that accounts for the special characteristics of ICs and their applications in order to deal with EOS in the design, handling and application of ICs.

2. Failure characteristics of ICs

The expectation of on-chip ESD protection to protect ICs not only from CL-ESD events but also from other kinds of electrical stress is often based on one or the other of the following assumptions:

(a) The current path within an IC is assumed to be the same for different kinds of electrical stress.
(b) The same part of an IC is assumed to be damaged regardless of the kind of electrical stress.
(c) Specific parts of an IC are assumed to respond equally to different kinds of electrical stress.
(d) The response of an IC to electrical stress is assumed to be independent of its mode of operation.
(e) The response of an IC to electrical stress is assumed to be proportional to the level of the given electrical stress.
(f) It is assumed that the responses of an IC to single kinds of electrical stress can be superimposed to give the response of the IC to superimposed electrical stresses.

As explained in [2], all these assumptions refer to characteristics of linear systems. Hence, the expectation of on-chip ESD protection to protect ICs not only from CL-ESD events but also from other kinds of electrical stress is typically based on the assumption that ICs are linear systems. Unfortunately, this assumption is generally wrong as will be explained in the following sections.

2.1. Semiconductor devices and ICs

As shown in [2], active devices (diodes, transistors and SCRs) are non-linear devices. This is the reason, why their electro-thermal characteristics are not analytically solved but are numerically simulated [7]. The non-linear characteristics of active devices become especially clear, by taking saturation, breakdown, snapback, hysteresis and memory effects into account. Especially ESD protection elements are typically driven deeply into breakdown, in order to clamp the voltage while conducting large currents. As explained in [8], their breakdown does not necessarily occur instantaneously as soon as a certain threshold voltage is exceeded but may be significantly delayed. The non-linearity of ESD protection devices is also confirmed by the lack of a common correlation between their HBM robustness and their SL-ESD robustness as reported in [1]. In fact, different ESD protection elements were found to have significantly different correlation factors, which makes it very difficult (if not impossible) to predict their response to other kinds of electrical stress.

Even passive devices like resistors, capacitors and inductors are known to show non-linear characteristics, if these devices are operated beyond their safe operating area, which may occur for any EOS [9,10]. Taking into account that almost all ICs employ both active and passive devices, it has to be concluded that ICs are generally non-linear systems.

2.2. Failure mechanisms

The failures caused by EOS can generally be divided into reversible (soft) and irreversible (hard) failures. A reversible failure can be removed by a functional reset (e.g. a power restart or a logic reset) or it can be healed by self-healing or physical treatment (e.g. annealing). Reversible failures are caused by electrical stress exceeding the trigger threshold of a functional failure mechanism (a switching operation, i.e. a non-linear mechanism) or by approaching the failure threshold (e.g. breakdown, another non-linear mechanism) of an IC component. Hence, the failure mechanisms causing reversible failures are non-linear.

Irreversible failures are permanent. They are either caused by electrical stress exceeding the trigger threshold of a physical failure mechanism (immediate failure) or by accelerated aging (delayed failure). The major failure mechanisms leading to irreversible failures caused by EOS are thermal overload due to dissipated energy and dielectric breakdown due to an electric field or voltage stress imposed for a certain amount of time [11]. As explained in [2,12], the relation between the thermal overload threshold of semiconductor devices and the stress time on the one hand and the relation between the time-to-failure and the