Microelectronics Reliability 54 (2014) 2471–2478

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Investigation of electromigration reliability of redistribution lines in wafer-level chip-scale packages

Chin-Li Kao [a,b], Tei-Chen Chen [a,*], Yi-Shao Lai [b], Ying-Ta Chiu [b]

[a] Department of Mechanical Engineering, National Cheng Kung University, Tainan 701, Taiwan
[b] Advanced Semiconductor Engineering, Inc. 26 Chin 3rd Rd., Nantze Export Processing Zone, Kaohsiung 811, Taiwan

ARTICLE INFO

Article history:
Received 29 March 2011
Received in revised form 22 April 2014
Accepted 23 April 2014
Available online 22 May 2014

Keywords:
Wafer-level chip-scale package (WLCSP)
Redistribution line (RDL)
Electromigration reliability

ABSTRACT

Wafer-level chip-scale packages (WLCSPs) have become subject to the same drive for miniaturization as all electronic packages. The I/O count is increasing and ball pitch is shrinking at the expense of trace pitch and in turn, current densities are increasing. This leads to current crowding and Joule heating in the vicinity of solder joints and under bump metallurgy (UBM) structures where resistance values change significantly. These phenomena are responsible for structural damage of redistribution line (RDL)/UBM and UBM/solder interconnects due to ionic diffusion or electromigration. In this work, sputtered Al and electroplated Cu RDLs were examined and quantified by three-dimensional electrothermal coupling analysis. Results provide a guideline for estimating maximum allowable currents and electromigration lifetime.

1. Introduction

Wafer-level chip-scale packages (WLCSPs) allow dice to be attached to printed circuit boards (PCB) without the use of underfill materials or prepackaging dice in larger packages like PBGA, QFP/QFN, etc. The elimination of the additional materials used in conventional packaging typically result in significant cost savings. There are limitations to the size of dice that can be mounted on PCBs due to the thermal expansion mismatch between die and PCB.

WLCSPs do have additional advantages: better electrical and thermal performance owing to the very short traces and solder interconnects. The WLCSPs come in three flavors: bump on die pad, bump on rebuilt die pad (repassivation of die pad with underlying dielectric layer), and bump on redistribution pad (original die pad is redistributed by sandwiching a fan-in trace between dielectric layers). The later enables a package with the most suitable bump pitch compatible with a cost-effective PCB. Furthermore, a wire bond die may be marketed in a wire bond package as well as a WLCSP.

The WLCSP have become subject to the same drive for miniaturization as all electronic packages. The I/O count is increasing, ball pitch is shrinking at the expense of trace pitch and in turn, current densities are increasing. This leads to current crowding and Joule heating in the vicinity of solder joints and under bump metallurgy (UBM) structures where resistance values change significantly [1]. These phenomena are responsible for structural damage of redistribution line (RDL)/under bump metallurgy (UBM) and UBM/solder interconnects due to ionic diffusion or electromigration.

Electromigration is a well-known phenomenon in flip-chip packages (e.g., [2,3]). For the die with RDL, the traces serve as electrical and thermal paths which lead to electromigration reliability concerns when current densities in the traces reach 100–1000 kA/cm^2 [4,5]. In this work, electromigration was examined for sputtered Al and electro-plated Cu RDL traces. The analysis was quantified by three-dimensional electrothermal coupling analysis. The calculated Joule heating effect was integrated into Black's equation to calibrate experimental electromigration lifetime. Results provide a useful guideline for estimating maximum allowable currents for RDLs with known dimensions.

2. Test vehicle and experimental set-up

The test vehicle consisted of a $4.4 \times 4.4 \times 0.43$ mm daisy-chained WLCSP mounted on a 1.0 mm thick eight-layer drop test board. The test vehicle had 98 I/Os with Sn–4.0Ag–0.5Cu solder joints, shown in Fig. 1. The drop test board was built according to the JEDEC regulation [6]. The non-solder mask defined (NSMD) Cu pads on the test board had a diameter of 240 μm, a pitch of 400 μm and were coated with organic solderability preservative (OSP). The solder joint diameter was 300 μm while the standoff after reflow was 200 μm. The diameter of the UBM was 240 μm and the polyimide opening was 210 μm. Two kinds of RDL and UBM types were evaluated in this study. The first RDL structure

* Corresponding author. Tel.: +886 6 2352973.
E-mail address: ctcx831@mail.ncku.edu.tw (T.-C. Chen).

http://dx.doi.org/10.1016/j.microrel.2014.04.014
0026-2714/

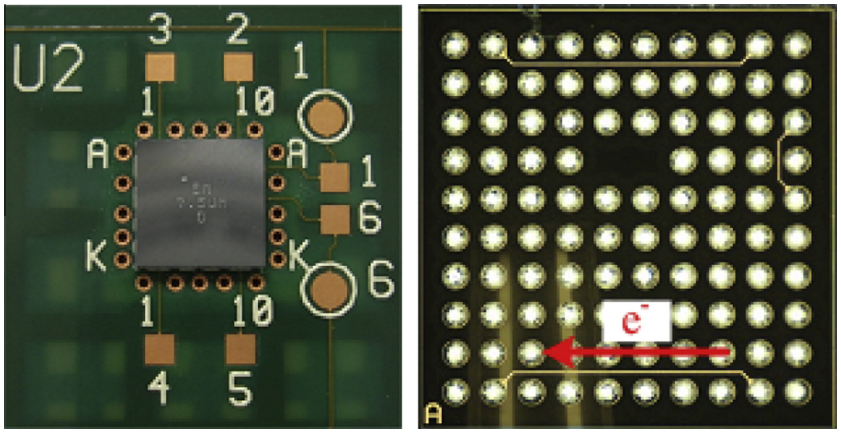

Fig. 1. Daisy-chained WLCSP test vehicle (left); electrons flow through single RDL (right).

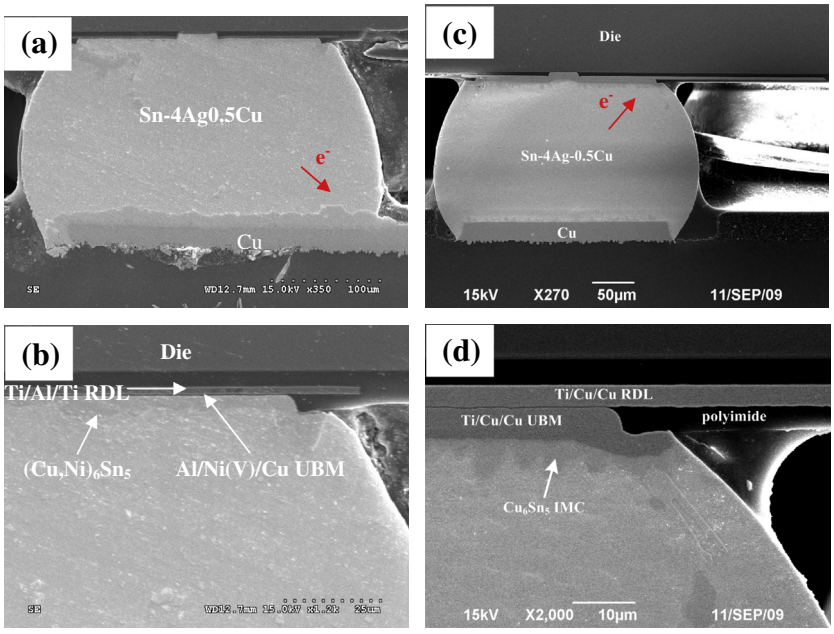

Fig. 2. SEM images of cross-sectioned WLCSP solder joint with (a and b) Ti/Al/Ti RDL and Al/Ni(V)/Cu UBM and (c and d) Ti/Cu/Cu RDL and Ti/Cu/Cu UBM.

was sputtered Ti/Al/Ti (0.2 μm/1.5 μm/0.2 μm) combined with a sputtered UBM: Al/Ni(V)/Cu (0.4 μm/0.325 μm/0.8 μm). The second RDL structure consisted of Ti/Cu/Cu (0.1 μm/0.2 μm/4, 6, or 7.5 μm electroplated Cu) combined with Ti/Cu/Cu UBM (0.1 μm/0.2 μm/8 μm electroplated Cu). Fig. 2 shows a scanning electron microscopy (SEM) image of a cross-sectioned WLCSP solder joint with the latter interconnect structure. Scallop-shaped Cu_6Sn_5 intermetallic compound (IMC) was formed along the Cu and solder interfaces at both the chip and board sides after reflow.

As shown in Fig. 1, only a single daisy chain at the edge of the die was powered with a constant DC electric current. Specimens were placed in a furnace to control the ambient temperature, T_{amb}. Electrical resistance of the particular daisy chain was monitored in situ during the test. According to JEDEC JEP154, the failure was determined whenever the circuit was resistance increases by 10% over its initial resistance.

3. Electrothermal coupling analysis and verifications

The electrothermal coupling analysis was carried out to provide current density and temperature fields of the RDL and solder joints of the WLCSP test vehicle. Governing equations for the static electric conduction and the steady-state thermal conduction are $\nabla \cdot \nabla\phi/\rho = 0$ and $\nabla \cdot k\nabla T = -\dot{q}$, respectively, where ρ denotes the electric resistivity, ϕ is the electric field, k is the coefficient of thermal conductivity, T is the temperature, and $\dot{q}$ is the heat flux.

The three-dimensional finite element model of the WLCSP test vehicle is shown in Fig. 3. In the finite element analysis, linear hexahedral electrothermal coupling elements were applied. The UBM was modeled as a single piece of Cu to simplify the analysis.

Table 1 lists coefficients of thermal conductivity and electrical resistivity for the constituent components of the WLCSP test vehicle. Note that thermal conductivity of the silicon die is a function of temperature. The test board was modeled as a laminate consisting of FR4 dielectric with eight layers of Cu, for which Cu was presumed to occupy 10% of each layer to account for the sparse trace layout. Through the measurement and calibration procedures developed by Lai and Kao [1], temperature-dependent electric resistivity of the solder joint, Al and Cu traces can be obtained, which are $121.8 + 0.375\ T$ μΩ-mm, $25.4 + 0.1\ T$ μΩ-mm, and $15.7 + 0.06\ T$ μΩ-mm, respectively, with T in Celsius. The components not given electric resistivities were assumed to be