Microelectronics Journal 52 (2016) 1–10

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

A 70.4 dB voltage gain, 2.3 dB NF, fully integrated multi-standard UHF receiver front-end in CMOS 130-nm

Carlos A.M. Costa Júnior [a], José B. Sales Filho [a], Gabriel C.L. Cunha [a], Diomadson R. Belfort [a], Sebastian Y.C. Catunda [a], Robson N. de Lima [b], Vincent P.M. Bourguet [a]

[a] UFRN, Campus Universitário, Lagoa Nova, CEP 59078-970, Natal/RN, Brasil
[b] UFBA, Rua Augusto Viana, s/n, Palácio da Reitoria, Canela, CEP 40110-909, Salvador/BA, Brasil

ARTICLE INFO

Article history:
Received 23 August 2015
Received in revised form
26 January 2016
Accepted 1 March 2016
Available online 21 March 2016

Keywords:
ARGOS
SBCDA
UHF receiver
CMOS
LNA
Mixer
Quadrature

ABSTRACT

The design of a fully integrated multi-standard UHF receiver front-end to be embedded in environmental data collection satellites is proposed. The circuit operates under the requirements of both SBCDA and the ARGOS 3. For that, the specifications of a multi-standard receiver front-end are firstly derived and then the implementation of a 70.4 dB voltage gain, 2.3 dB NF, 48 mW energy consumption, single-ended input and differential quadrature output receiver front-end in 130-nm CMOS standard technology is presented. The design is validated through post-layout simulation.

1. Introduction

Remote environments are mainly monitored by low orbit satellites, which acquire environmental information from automatic data collection platforms (DCPs) spread around the desired research locations. Due to the need of updating the Brazilian Environmental Data Collection System (SBCDA), a pioneer project for using a nano-satellite constellation to replace the outdated current SBCDA satellites has been proposed [1]. Therefore, more compact, yet reliable and retro-compatible on-board systems are desired.

A general Environmental Data Collection System (EDCS) is divided into three segments, the space one, formed by the data collection satellites (DCS), and two ground ones, the DCPs and the receiving ground station. The platforms collect the environmental data and broadcast them to satellites containing on-board transponders. The collected data is then sent to a ground station, which processes and stores the information in a database for user access. Examples of successful data collection systems are the SBCDA and the French-American ARGOS.

The design of radio frequency electronic systems for space applications, as the EDCS, presents some challenges. (1) The signal attenuation and the interference susceptibility caused due to the long distance between satellites and DCPs; (2) the limited amount of available on-board power; and (3) the radiation effects. The latter, however, may be overlooked when designing analog integrated circuits for nano-satellites systems, since the design of such systems already foresees the use of non radiation-hardened components, in order to speed up its construction and reduce considerably the overall cost [2]. To cope with the aforementioned constraints, a receiver front-end of an EDCS transponder should be able to handle power limited signals with a good sensitivity and good selectivity. The system power, although not specified, is desired to be kept as low as possible.

The current SBCDA transponder, built in 1993, uses a superheterodyne architecture (shown in Fig. 1a), widely employed in older satellite systems to ensure the stringent requirements. Its good performance, high gain and 3.5 dB NF [3], is reached by means of several steps of amplification, mixing and filtering. However, this numerous amount of steps and its need for bulky image rejection filters hardens its full integration [4]. Moreover, the actual transponder does not allow any Digital Signal Processing (DSP) and it occupies a volume of 5645 cm^3, therefore not suitable to be embedded in nano-satellites, which usually have a total volume of 1000 cm^3. Thus, to allow full integration, a quadrature low IF receiver architecture can be used. It does not suffer

E-mail address: carlos.mendes@ct.ufrn.br (C.A.M.C. Júnior).

http://dx.doi.org/10.1016/j.mejo.2016.03.001
0026-2692/

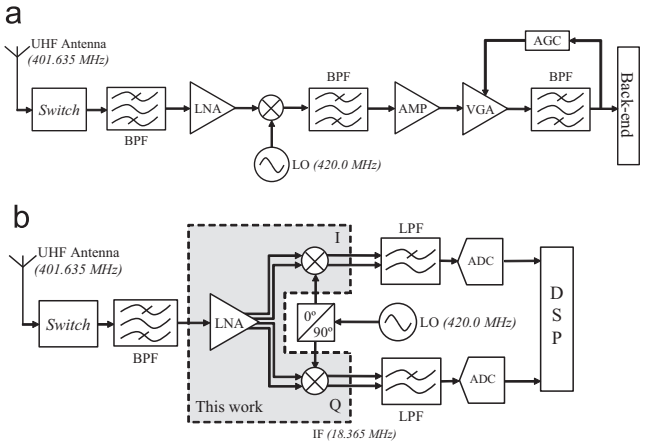

Fig. 1. Receiver front-end architectures. (a) Current Super-Heterodyne architecture. It is fully analog and uses discrete components. (b) Proposed Low-IF architecture. The dotted line highlights the fully integrated receiver front-end presented in this work.

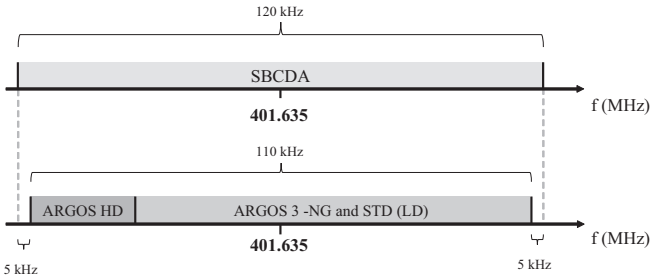

Fig. 2. SBCDA and ARGOS 3 bandwidth requirements. In order to cover both standards this work considers a 120 kHz bandwidth around 401.635 MHz.

from DC offset or flicker noise issues as the zero-IF does and, in addition, it mitigates the image frequency [5].

In this work, the design of a fully integrated CMOS UHF receiver front-end in a low-IF architecture is presented (Fig. 1b). The front-end consists of a 4-stage single-end input and differential output LNA and a differential quadrature mixer.

This paper is organized as follows. Section 2 presents the specifications for a multi-standard receiver front-end compatible with SCBDA and ARGOS 3. Section 3 discuses the topologies of the single-to-differential LNA and the quadrature mixers. The circuits implementation is presented in Section 4. Schematic and post-layout simulation results along with comparison with the state-of-the-art works are shown in Section 5. Finally, conclusions and discussions are presented in Section 6.

2. Receiver system-level considerations

2.1. Summary of the multi-standard front-end requirements

The objective of implementing a fully integrated receiver front-end for SBCDA satellites can be extended to co-work with the ARGOS 3 due to the superposition of their bandwidths, resulting in a 120 kHz bandwidth around 401.635 MHz as shown in Fig. 2. The only concern is to have the front-end requirements fulfilling both systems.

ARGOS 3 is divided into two categories, the High Data Rate (HD) and the Low Data Rate (LD), where the latter is sub-divided into Low Power (New Generation, NG) and Standard (STD). Both LD categories transmit at a data-rate of 400 bit/s, but differ in power transmission and applications. The NG category allows itself to be more compact than the STD one, thus it can be used by size-constrained platforms, such as ones employed in wild animals [6]. The HD has a data rate of 4800 bit/s and it is used for applications requiring larger amount of information. The SBCDA presents basically the same features as the STD.

Table 1
Summary of the multi-standard front-end requirements.

Parameters	SBCDA	ARGOS-3 LD		ARGOS-3 HD	FINAL
		STD	NG		
NF FE (dB)	11.0	11.0	**4.3**	6.5	**4.3**
Power Gain (dB)	39.3	39.3	**49.0**	41.0	**49.0**
Sensitivity (dBm)	−124.5	−124.5	**−138.5**	−124.5	**−138.5**
Max. input (dBm)	**−99.5**	−115.5	−115.5	−109.5	**−99.5**
Signal BW (Hz)	1000	1000	500	1920	–
iCP1 (dBm)	−82.5	−82.5	−82.5	−82.5	**−82.5**
IIP3 (dBm)	−72.9	−72.9	−72.9	−72.9	**−72.9**

In [7] the specifications for all four standards mentioned above were considered and the front-end requirements were derived for each category and are summarized in Table 1. The column FINAL gathers all the requirements needed for a mutually compatible SBCDA-ARGOS receiver front-end.

2.2. LNA and mixer requirements

The LNA is designed to reach or to overcome already published high gain UHF LNA performances, such as an NF of 2.1 dB and a energy consumption of 22 mW, as presented in [8]. Considering this goal reachable, the mixer requirements can be derived as follows:

2.2.1. Gain

In order to assure a low noise front-end, all the required front-end power gain (49 dB) will be provided by the LNA. As it is normally a challenge to concentrate such a high gain in a LNA, it is desired to use an active mixer instead of a passive one to avoid any power degradation that the latter would cause. By doing so, it guarantees that the on-silicon implementation will reach the required overall gain.

2.2.2. Noise figure

Considering the front-end consists of a LNA and a mixer, the total noise factor of the system is given by [5]:

$$F_{FE} = F_{LNA} + (F_{MIX} - 1)/G_{LNA}, \quad (1)$$

where G_{LNA} is the gain of the LNA and F_{FE}, F_{LNA} and F_{MIX} are respectively the noise factor of the front-end, the LNA and the mixer, respectively.

From [8] it is possible to infer that a noise figure of 2.1 dB can be reached for an high gain UHF LNA. Thus, it is possible to compute the mixer noise factor as

$$F_{MIX} = 1 + G_{LNA}(F_{FE} - F_{LNA}) = 84,972.25. \quad (2a)$$

$$NF_{MIX} = 10\log(84,972.25) = \mathbf{49.3\ dB}. \quad (2b)$$

Therefore, a mixer noise figure of less than 49.3 dB is a feasible requirement to be reached in order to ensure the overall NF of less than 4.3 dB.

2.2.3. Linearity

The LNA IIP3 is obtained by counterweighting the IIP3 value from the LNA reference [8] (−74 dBm) to the required front-end gain (49 dB), resulting in a equivalent IIP3 of −64.75 dBm. The