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High performance current mirrors using quasi-floating bulk

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ABSTRACT

In this paper, a modified structure of standard MOSFET is proposed which offer high transconductance in comparison to its conventional architecture. The conventional MOSFET is a four terminal device whose fourth terminal, the bulk is connected to either negative/positive supply for N-channel/P-channel transistor respectively, or to their source terminal. In the proposed structure, instead of connecting bulk to supply rails or to source terminals, the bulk is configured in a quasi-floating state and then connected back to its gate terminal. The resultant is a gate driven quasi floating bulk MOSFET. Under DC analysis, the proposed structure operates as standard gate driven MOSFET whereas performing analysis in frequency domain the structure results in effective transconductance higher than that of standard MOSFET. Using the proposed structure, three high performance current mirrors are presented in this paper which showed improved performance over its conventional architectures. Performance of the proposed structure and the current mirror circuits are verified using HSpice simulations on 0.18 μ m mixed-mode twin-well technology at a supply voltage of ± 0.5 V.

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1. Introduction

The demand of low power high performance portable light weight electronic and implanted medical devices has been increasing in an exponential manner. The traditional approach followed to fulfill such demand is achieved through scaling of device geometry and proportionally the supply voltage in deep sub-micron technology [1]. However, the scaling of supply voltage has its limitation due to presence of threshold voltage of MOSFET which degrades the lifespan of battery-operated devices. In context to this the research has been forced to use non-conventional techniques to realize the threshold free circuits from its input signal path but at the cost of degraded characteristics compared to standard gate-driven (GD) MOSFET. Moreover, low threshold MOSFET also increases the chances of leakage current. Some of well-known widely used non-conventional techniques for realizing low voltage circuits are named as bulk-driven (BD) [2–5], floating and quasi-floating gate (FG and QFG) [6–8], bulk-driven floating and quasi-floating gate (BD-FG and BD-OFG) [9–16]. Each of the aforementioned technique has its importance in specific field. Another approach to resolve threshold limitation with enhanced performance was observed in dynamic threshold

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http://dx.doi.org/10.1016/j.mejo.2016.02.012 0026-2692/© 2016 Elsevier Ltd. All rights reserved. MOSFET (DTMOS) where gate is connected to the bulk [17]. It gives the combined advantage of GD and BD MOSFET. However, circuits based on DTMOS has limitation of working at higher supply voltage, i.e. greater than 0.4 V to avoid latch up which is caused by turning-on of lateral npn and pnp parasitic bipolar transistors [18,19]. Such latch up can results in very high body currents and device may not perform accurately. In context to this, the structure of MOSFET proposed is modified by transforming the bulk in quasi floating state and connecting back to its respective gate. The structure formed is named as gate-driven guasi-floating bulk (GD-QFB) MOSFET. Under DC conditions, the proposed structure behaves as standard gate-driven MOSFET whereas while performing the small-signal analysis the structure results in high transconductance over GD MOSFET, i.e. addition of gate transconductance and scaled body transconductance. The adverse effect observed in proposed structure is the increased parasitic capacitance i.e. effect of bulk capacitance also gets added up in calculation of effective transconductance. However, using high value input capacitors compared to bulk and gate capacitance the GD-QFB leads to high transconductance and the degraded frequency performance caused by increased parasitic effect becomes negligible comparatively. Also as observed under DC conditions the proposed structure acts like standard GD MOSFET so there exist no latch-up constraint and the architecture based on GD-QFB MOST can be made to operate at any desired supply voltage. The advantage and disadvantage of GD-QFB MOST is shown with the help of three high performance current mirror circuits proposed in this paper.

Current mirror is the basic building block for analog circuits whose primary function is to copy the input current to its high impedance output node. The commonly used applications of current mirror can be seen in level shifting, biasing, active loading, etc. [20,21]. Hence, design of high performance current mirror is the key requirement of analog circuits. The high performance here is defined in terms of wide current driving capability, high linearity, low input and high output resistances, and high bandwidth. The paper presents a high bandwidth, low input impedance cascode and self-biased high swing cascode current mirror based on GD-QFB MOSFET. Also an improved performance in terms of input and output impedance of recently proposed low power current mirror is observed by applying the GD-QFB technique. The paper is divided in five sections. Section 2 covers the detail of proposed GD-QFB MOSFET and its simulations so as to have a fair performance comparison with parameters of standard MOSFET. Section 3 details the proposed three high performance current mirrors realization using GD-QFB MOSFET. The simulation results are discussed in Section 4 and finally the paper is concluded in Section 5.

2. Proposed GD-QFB MOSFET

The schematic of proposed N-channel GD-QFB MOSFET along with its parasitic capacitances is shown in Fig. 1(a) and its symbol in Fig. 1(b).

In Fig. 1(a), the MOS transistor *M*1 is configured in GD-QFB mode. The bulk is transformed in quasi-floating state via input capacitor C_{in} and high value resistor R_{large} whose realization is done using N-channel MOST *MN* working in cut-off mode by connecting its gate to negative supply rail VSS. Similarly for the P-channel GD-QFB, the high value resistance is realized using P-channel MOST with its gate connected to positive supply VDD. The effective quasi floating bulk potential under ac in s-domain is expressed as

$$V_{qfb} = \left(\frac{sR_{large}C_{T,qfb}}{1 + sR_{large}C_{T,qfb}}\right) \left(\frac{(C_{in} + C_{qfbg})V_{in} + C_{qfbd}V_D + C_{qfbs}V_S}{C_{T,qfb}}\right)$$
(1)

where C_{qfbg} , C_{qfbd} , C_{qfbs} are the associated parasitic of NMOST *M*1 to the floating bulk, $C_{T,qfb} = C_{in} + C_{qfbg} + C_{qfbd} + C_{qfbs} + C_{gd,MN}$ is the total effective capacitance seen from floating bulk and $C_{gd,MN}$ is the parasitic capacitance associated with NMOST *MN*. Under DC conditions, the input capacitor becomes open circuit and the device



Fig. 1. (a) N-channel GD-QFB MOSFET and (b) symbol.

operates as standard GD NMOST whereas for small-signal analysis the proposed structure results in effective transconductance higher than standard GD NMOST, i.e. sum of gate and scaled body transconductance.

The detailed analysis of GD-QFB NMOST basic parameters in saturation mode is shown below. Also correspondingly to parameters explained the simulations are performed with GD MOST parameters achieved under the same environment for fair comparison. For simulation the NMOST M1 having width and length of 100 μ m and 0.54 μ m, respectively operated at a supply of 0.5 V using UMC 0.18 μ m technology with the help of HSpice simulator. The other assumed parameters for simulation are $C_{in} = 1$ pf while the width and length of *MN* (for realizing R_{large}) is taken as 0.36 μ m and 0.36 μ m, respectively.

2.1. Transconductance

The drain-to-source current in saturation region is given by

$$I_{DSsat.} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th,qfb})^2$$
⁽²⁾

where $V_{th,qfb} = V_{th0} + \gamma \left(\sqrt{\left| 2\phi_f \right| + \left(V_s - V_{qfb} \right) - \left| 2\phi_f \right|} \right)$ Taking derivative of (2) with respect to input voltage

$$g_{m,GDQFB} = g_m + \left(-\frac{C_{in} + C_{qfbg}}{C_{T,qfb}}\right) \left(\frac{-\gamma}{2\sqrt{\left|2\phi_f\right| + V_{SB}}}\right) g_m$$
(3)

Hence the effective transconductance of GD-QFB NMOST is given as

$$g_{mb,GDQFB} = g_m + \left(\frac{C_{in} + C_{qfbg}}{C_{T,qfb}}\right) g_{mb}$$
(4)

where g_m and g_{mb} is the gate transconductance and body transconductance of standard NMOST. The simulation of comparison of transconductance of GD-QFB to GD NMOST is shown in Fig. 2. As observed in case of GD-QFB the addition of scaled body transconductance results in effective transconductance of 5.4 mA/V higher than GD MOSFET which is 4 mA/V.



Fig. 2. Transconductance plot for GD and GD-QFB NMOST.

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