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Design of a fully integrated receiver analog baseband chain for 2.4-GHz ZigBee applications

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ABSTRACT

A receiver analog baseband (ABB) chain for an integrated ZigBee (IEEE 802.15.4) transceiver is presented in this paper. The ABB is composed by a 3rd-order complex band-pass filter (BPF), a variable gain amplifier (VGA) and an analog-to-digital converter (ADC). The circuit topology of each building block has been designed complying with the IEEE 802.15.4 standard as well as featuring low power consumption and small chip size. In this work, a mixed-signal frequency auto-tuning scheme is proposed for complex BPF to accommodate the performance deterioration due to the process, voltage and temperature (PVT) variations. A novel method combined opamp- and capacitor-sharing is presented for ADC to obtain low power consumption and elimination of memory effect. The proposed ABB demonstrates 70 dB dynamic range by 2 dB/step, 12 dBm IIP3 and 35.2 nV/$\sqrt{}$Hz input referred noise. The measured SNDR and SFDR are 41.9 dB and 58.7 dB, respectively. Implemented in a standard 0.18-μm CMOS technology, the entire receiver ABB chain occupies an area as small as 1.5 mm^2 and the total power consumption is only 16 mW at max gain setting from a 1.8 V supply.

1. Introduction

Recently, the low-power single-chip transceiver has drawn great attention duo to the demand of longer battery life and lower cost of mobile communication devices [1,2]. ZigBee (IEEE 802.15.4) has become a primary solution for high density of nodes and simple protocol which is established as low-complexity, low-cost, and low-power short-range wireless connectivity [3,4].

The receiver analog baseband (ABB) chain serves as a crucial component for the transceiver or even the one of the most key building blocks especially for power-limited ZigBee standard since it typically consumes several milliwatts to tens of milliwatts, which accounts for a significant share of total receiver power consumption. Although many literatures discussed the implementation of the wireless receiver analog baseband (ABB) [5–7], few of them aim at the ZigBee applications. Moreover, most of them are introduced without analog-to-digital converter (ADC) block, which cannot be neglected for operating as a critical interface circuit and servicing at the intermediate frequency (IF) as same as other ABB blocks.

This paper presents the design and implementation of the receiver analog baseband (ABB) chain for 2.4-GHz band ZigBee transceiver in a standard 0.18-μm CMOS technology. The ABB is implemented in low-IF architecture which consists of a complex band-pass filter (BPF), a variable gain amplifier (VGA) and an analog-to-digital converter (ADC). With the prime targets of low complexity, small chip area and low power, trade-off has been made over the design boundaries and circuit topologies of the different building blocks to optimize the overall ABB performance. Furthermore, a mixed-signal automatic frequency tuning scheme is proposed for BPF to ensure the frequency response accurately. An evaluation-time-sharing (ETS) technique which combined opamp- and capacitor-sharing is employed for ADC for low-power consumption and removing memory effect. The receiver architecture and specifications are presented in Section 2. Section 3 describes in detail about the design of the ABB chain. The experimental results are reported in Section 4 and conclusions are presented in Section 5.

2. Architecture and specifications

Fig. 1 shows the low-IF ZigBee receiver with the emphasis on the ABB chain including BPF, VGA and ADC. From the view of receiver system, considering the effect of RF front-end (LNA+Mixer), the noise figure (NF) and input 3rd order intercept point (IIP3) assigned for BPF+VGA are 38 dB and 11 dBm, respectively. The BPF specifications can be derived from the requirements of jamming resistance. Since the IEEE 802.15.4 standard [8] defines 16 channels between 2.405 GHz and 2.48 GHz

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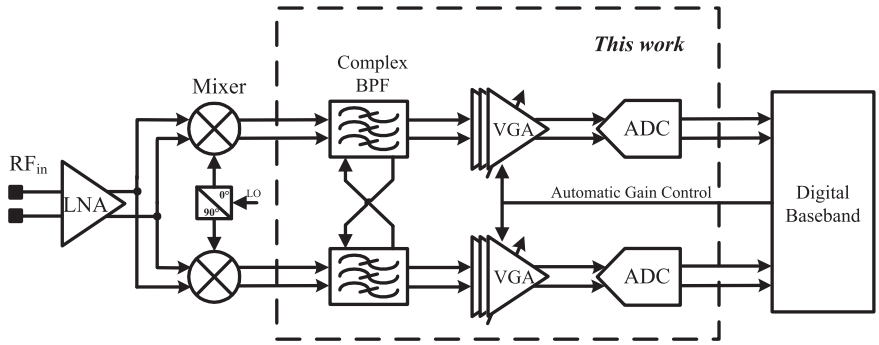

Fig. 1. Block diagram of the low-IF ZigBee receiver.

with a bandwidth of 2 MHz and a channel spacing of 5 MHz, the requirements on bandwidth can be chosen as 3 MHz. Furthermore, the PHY requires 0 dB rejection at the adjacent channel and 30 dB rejection at the alternate channel, respectively. Therefore, assuming 10 dB margins, 10 dB adjacent channel rejection and 40 dB alternate channel rejection are enough for BPF design. To achieve a proper signal strength, according to IEEE 802.15.4 standard, the ZigBee receiver chain should achieve a dynamic range of about 95 dB assuming a 10 dB margin to meet the −85 dBm sensitivity requirement [9]. Assigning the RF front-end gain of 25 dB, the ABB shall provide the maximum gain of 70 dB with the gain step of 2 dB. The requirements of ADC can be derived as follows. The integral non-linearity (INL) and differential non-linearity (DNL) are required less than 1 LSB to guarantee the monotonicity. Furthermore, the loss of receiver signal-to-noise ratio (SNR) contributed by ADC can be acceptable if the SNR of the ADC is 20 dB higher than the SNR due to the thermal noise component [10]. Considering the receiver noise power of −90.5 dBm and the processing gain of 9 dB, the required SNR for ADC is 16.5 dB which means the required effective number of bits (ENOB) is 3 bits. Assuming the channel interferer power is −30 dBm, which results in additional 1 bit resolution to fit the interferer. Moreover, another 3 bits is for design margin with considerations for discontinuous gain of VGA and modulation effect in digital baseband. Finally, a total resolution of 7 bits and an oversampling clock frequency of 16 MHz are chosen for ADC. The specifications of each ABB block are summarized in Table 1.

Table 1
Summary of receiver ABB specifications.

Modules	Parameters	Standard specifications	Target specifications
BPF	Gain	–	0 dB
	Bandwidth	–	3 MHz
	Adjacent channel attenuation	> 0 dB	10 dB
	Alternate channel attenuation	> 30 dB	40 dB
VGA	Dynamic range	> 60 dB	70 dB
	Gain step	–	2 dB
ADC	Resolution	> 4 bit	7 bit
	Sample frequency	–	16 MS/s
	INL /DNL	–	< 1 LSB

3. Circuit design

3.1. Complex BPF

For the low-IF structure receiver, the inescapable drawback is the image interference. After quadrature down-mixer, the image signal (centered at ω_{-IF}) and desired signal (centered at ω_{IF}) located around zero frequency symmetrically. The image signal could be considered as a strong co-channel interference that should be eliminated. Therefore, a complex band-pass filter followed the mixer is adopted for passing the desired signal and rejecting the unwanted image as well as the neighbor channel interferers.

Complex BPF design can be achieved by applying the transformation $s \rightarrow s - j\omega_{IF}$ to the transfer function of real low-pass filter (LPF) [11]. The Butterworth approximation is chosen in this paper since the relatively relaxed attenuation requirements indicated in Section 2. Furthermore, compared with Chebyshev and Elliptic approximations, Butterworth approximation is preferred owing to the best group delay (i.e. the lowest distortion) which could relax the design requirements of following part. The order N and the attenuation A_{dB} for a LPF Butterworth approximation fulfils:

$$A_{dB} = 10 \log \left[1 + \left(\frac{f_x}{f_c} \right)^{2N} \right] \tag{1}$$

where f_x and f_c are the frequency and cut-off frequency, respectively. According to Table 1, the two attenuation requirements can be described as:

$$\left.\begin{aligned} 10 &= 10 \log \left[1 + \left(\tfrac{5}{1.5} \right)^{2N} \right] \\ 40 &= 10 \log \left[1 + \left(\tfrac{10}{1.5} \right)^{2N} \right] \end{aligned}\right\} \quad \Rightarrow \quad N = 3 \tag{2}$$

Thus a 3rd-order filter would be sufficient in this paper which could be realized by three cascaded 1st-order filters. The transfer function of an ideal 3rd-order Butterworth LPF can be given by:

$$\begin{aligned} H_{LP}(s) &= A \left(\frac{FSF.p_1}{s + FSF \cdot p_1} \times \frac{FSF.p_2}{s + FSF \cdot p_2} \times \frac{FSF.p_3}{s + FSF \cdot p_3} \right) \\ &= A \frac{FSF^3}{s^3 + 2FSF \cdot s^2 + 2FSF^2 \cdot s + FSF^3} \end{aligned} \tag{3}$$

where A is the dc gain and FSF is the Frequency-Scaling Factor of $2\pi f_c$. p_1, p_2 and p_3 are the poles of the 3rd-order LPF with a bandwidth of 1 rad/s and respectively given by:

$$p_1 = 0.5 + 0.866j \;\; p_2 = 0.5 - 0.886j \;\; p_3 = 1 \tag{4}$$

Then the transfer function of the "transformed" complex BPF by $s \rightarrow s - j\omega_{IF}$ can be expressed as:

$$\begin{aligned} H_{CBP}(s) &= A \frac{FSF^3}{(s - j\omega_{IF})^3 + 2FSF(s - j\omega_{IF})^2 + 2FSF^2(s - j\omega_{IF}) + FSF^3} \\ &= A \left(\frac{FSF}{(s - j\omega_{IF}) + FSF \cdot p_1} \times \frac{FSF}{(s - j\omega_{IF}) + FSF \cdot p_2} \times \frac{FSF}{(s - j\omega_{IF}) + FSF \cdot p_3} \right) \end{aligned} \tag{5}$$