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Improvements on thermal stability of graphene and top gate graphene transistors by Ar annealing

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ABSTRACT

Thermal annealing of graphene was studied to improve the thermal stability. During the annealing under an Ar atmosphere with temperature from 100 °C to 600 °C, graphene exhibits partial removal of PMMA residues, low density of defect cracks in SEM images and relatively low I_D/I_G ratios in Raman spectrum probing. For a top-gated graphene transistor with thermal annealing, it performs high carrier mobility up to 3500 $cm^2 V^{-1} s^{-1}$ and slightly asymmetric bipolar behaviours as well as slight Dirac point variation within ±0.2 V.

1. Introduction

Since its discovery, graphene has attracted much attention for application in electronic devices because of its outstanding characteristics such as transparency, mechanical strength, and ballistic transportation [1,2]. As a promising candidate for one of the next-generation electronic materials, graphene has been highly developed in the past few years [3,4]. Despite all the developments in graphene and graphene electronic devices, the thermal stability of graphene is rarely mentioned, however. Although suspended graphene exhibits thermal stability up to 2600 K [5], graphene deposited on a silicon dioxide film on a silicon wafer, the most commonly used substrate for graphene, has a much lower thermal stability because of the large mismatch between the thermal expansion coefficients of graphene and silicon dioxide [6]. When the temperature increases, the SiO_2/Si substrate expands while graphene contracts. At the interface between graphene and SiO_2/Si, the opposing expansion stress may cause surface tension, defects, disorder, or even cracking. Nan et al. systematically investigated the thermal stability of monolayer and bilayer exfoliated graphene and graphene prepared by chemical vapor deposition (CVD) on silicon dioxide in air using probing Raman spectroscopy [7]. Unfortunately, they did not demonstrate thermal stability in the electrical characteristics of graphene. Moreover, graphene will be packaged to protect it from oxygen doping in integrated circuit (IC) fabrication. Thus, the following topics should be considered when investigating the thermal stability of graphene for electronic applications: a) Joule heating caused by high aggregation carrier density (for example, the temperature of graphene nanoribbons (GNRs) is increased to 300 °C at a drain–source voltage of $V_{DS} = 2$ V) [8,9]; b) high-*k* top-gated dielectric thin-film formation on graphene through thermally assisted atomic layer deposition (ALD) [10], and further annealing of high-*k* materials [11] for smooth morphology, lower trap density, removal of charged impurities, or to obtain higher equivalent oxide thickness; c) high-temperature annealing in the presence of specific gases (for example, H_2S [12] and NH_3 [13]) for graphene doping. Moreover, the development of heterojunction structures like the gate-controlled Schottky barrier between graphene and silicon has resulted in logic device performances that are comparable to those of metal–oxide–silicon (MOS) field-effect transistors (FETs) [14], whose fabrication require

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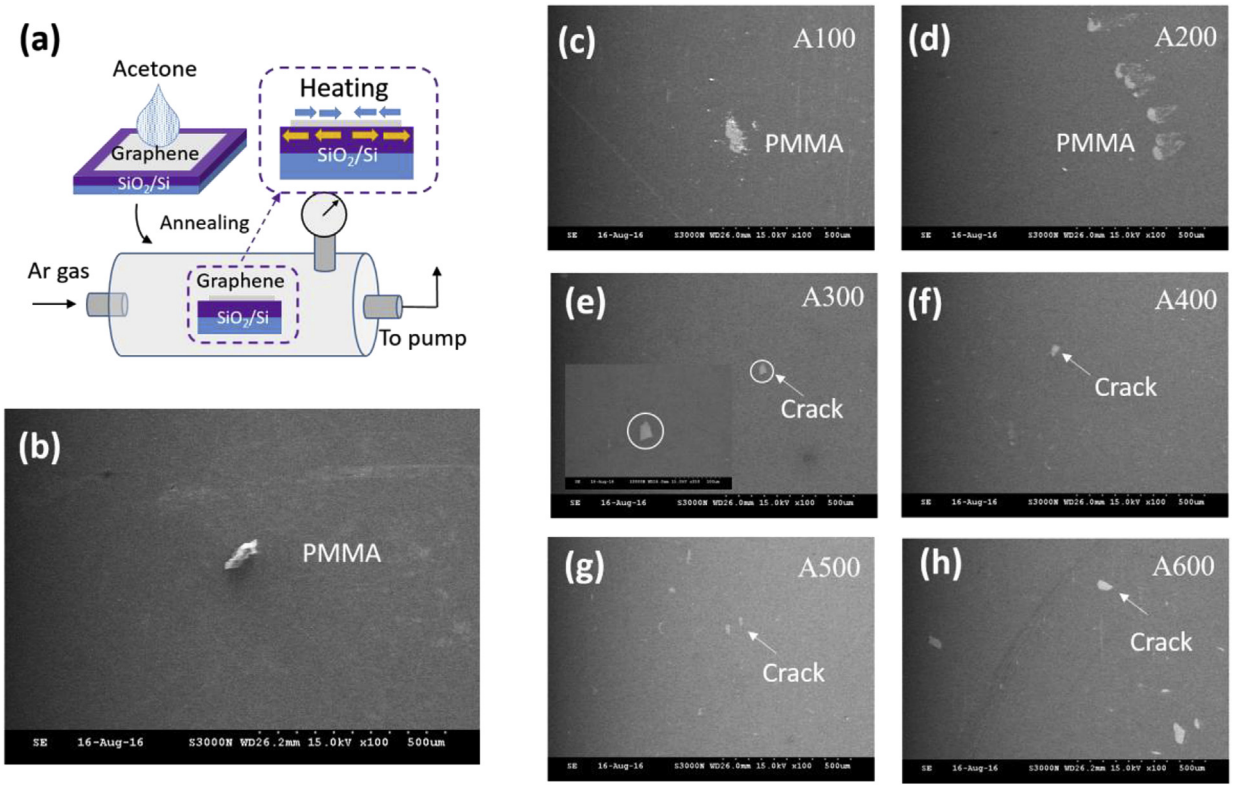

Fig. 1. (a) Illustration of experimental setup for studying the thermal stability of graphene on a SiO_2/Si substrate. SEM image of (b) as-transferred graphene and graphene after annealing at (c) 100 °C, (d) 200 °C, (e) 300 °C, (f) 400 °C, (g) 500 °C, and (h) 600 °C. Scale bar: 500 μm. The inset of (e) shows the enlarged SEM image of the crack, scale bar: 100 μm.

high-temperature processes such as the formation of Ni silicide for lowering the source–drain contact resistant of silicon [15].

We studied the thermal stability of CVD graphene that was transferred onto SiO_2/Si substrates only up to 600 °C due to the prevention of carbon reduction reaction with underneath SiO_2 [16]. An Ar gas atmosphere could suppress the formation of amorphous carbons through PMMA residue carbonization, comparing to other annealing conditions (including H_2, H_2/Ar, and vacuum) [17]. The thermal stability of graphene was comprehensively analyzed by scanning electron microscopy (SEM), Raman spectroscopy, and electrical characterization of graphene FETs. Comparing with previous study, Ar annealing on top-gated graphene transistors improves the thermal stability significantly. This study evaluates the thermal stability of graphene for application in FETs; the results show that graphene under Ar annealing is suitable for high-temperature IC fabrication processes.

2. Experiment

2.1. Graphene preparation

Cu foils were loaded into a low-pressure (below 2.5 mbar) chemical vapor deposition (CVD) furnace and heated to 1000 °C under a H_2 flow at 50 standard cubic centimeters per minute (sccm, cm^3/min) to remove the native Cu oxide. After 30 min annealing, CH_4 was introduced at 1 cm^3/min to grow graphene on the Cu foils for 20 min. The furnace was then cooled to room temperature at a rate of ~5 °C/s. A layer of poly-methyl methacrylate (PMMA) was spin-coated onto the graphene on Cu. The films were then treated with a Cu etchant and rinsed with deionized (DI) water before they were transferred to the SiO_2/Si substrates. The PMMA supporting layer was removed from each film by acetone and the remaining graphene films were rinsed with isopropyl alcohol. The SiO_2/Si substrates were pretreated by immersing them in a H_2SO_4/H_2O_2 (3:1) solution to remove organic residues on the surface.

2.2. Graphene annealing

The as-transferred graphene films on SiO_2/Si substrates were loaded into the furnace chamber. The chamber was evacuated to a low pressure (below 2.5 mbar) to exclude oxygen and then Ar gas was injected to maintain an atmosphere for annealing. All samples were heated to their respective specified temperature and then cooled to room temperature at a rate of ~5 °C/s.

2.3. Raman spectroscopy and mapping

Raman spectra were obtained using laser excitation at a wavelength of 473 nm (photon energy: 2.62 eV); the laser beam was focused to a spot with size of 0.5 μm. The Raman peak of Si at 520 cm^{-1} was used as the calibration signal for graphene probing. For the Raman mapping, each sample was scanned in areas measuring 2 mm × 2 mm, with a step size of 200 μm to avoid localized thermal aggregation induced by the incident laser energy.

2.4. Fabrication of top-gated field-effect transistors

The graphene transistors were fabricated by traditional lithography as follows: (i) 50-nm Ni source and drain contacts were formed on graphene by thermal deposition; (ii) the graphene channel was defined by O_2 plasma etching; (iii) thermal deposition of 150-nm Al to form the top gate and 5-nm AlO_x layer to form the gate dielectric [18].