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A new kind of vertically aligned field emission transistor with a cylindrical vacuum channel

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ABSTRACT

This study investigated a vertically aligned field emission transistor with a cylindrical vacuum channel. The channel length of this proposed transistor can be precisely controlled and easily fabricated to be comparable to the mean free path of electrons in air so that the device can operate in the air without performance degradation. In the study, this vacuum transistor showed a low threshold voltage (1.2 V, 2.2 V, and 3.3 V) with a gate dielectric thickness of 10 nm, 15 nm, and 20 nm and a subthreshold slope of 1.1 V/dec. It was found that the vacuum channel radius should be no less than 20 nm, otherwise, severe performance degradation will appear due to the effect of the gate shield (leading to reduction of the anode current) and electron collision events with the dielectric layer (presenting reliability issues). This kind of vacuum transistor may have wide applications in extreme conditions such as high temperature and intense irradiation.

1. Introduction

Vacuum electronic devices based on ballistic transport of electrons possess outstanding performance in amplifying, switching, and modulating electrical signals. In vacuum electronic devices, electrons transport in vacuum channels without electron scattering. The electron transport velocity is several times greater in magnitude than that during transmission via semiconductors. Moreover, vacuum devices are more suitable for application in harsh operational conditions such as high temperatures and irradiated environments. However, it has been several decades since vacuum tubes were replaced by solid state devices [1]. The main advantages of solid state devices are low fabrication costs, high energy efficiency, and their long lifespan, as well as their ideal form for integrated circuits (ICs). To date, researchers have dedicated much effort to adopting semiconductor manufacturing technology for fabrication and to scaling back on vacuum electronic devices [2–6]. However, to obtain a high conducting current, the distance between a cathode and anode needs to be at the magnitude of submicrometers or even nanometers. This requires an elaborate and complicated semiconductor fabrication process with no guarantee of a high-quality cathode since the reliability and lifetime of the spike type cathode may be a problem, and the length of the channel between the cathode and anode cannot be precisely controlled [5,6].

Recently, a new kind of vacuum field-effect transistor (VFET) with a vertically aligned structure has been reported [7–12]. In this vertical structure, the channel length between the anode and cathode is determined precisely by the thickness of the oxide layer and is designed to be smaller than the mean free path of electrons in air. Thus, the VFET can be operated under atmospheric pressure without performance degradation. However, research focusing on the vertically aligned transistor has been very limited so far, and the working principle remains ambiguous. In this work, we propose a vertically aligned vacuum field-effect transistor with a cylindrical void channel. The cathode and gate of this transistor possess an annular ring structure. Therefore, the electron emission surface has a completely consistent state, and, consequently, the electric field on the emission surface and the density of electrons concentrated near the cathode edge are uniform. This characteristic may effectively reduce device failure resulting from extremely intense local electrical fields on the emission surface due to the inhomogeneous electrical field distribution when relatively high gate or anode voltage is applied [13,14]. Moreover, the cylindrical void channel makes it easier to investigate the issues of reliability as well as how to minimize the impact of the gate shield effect, both of which are

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related to channel size. In this study, we explored the performance of the proposed transistor by numerically investigating the influence of different geometry parameters (e.g., gate dielectric thickness and vacuum channel radius) on behavior characteristics. We hope that the results may help in understanding the working principle and facilitating the improvement of such devices.

2. Device structure and basic working principle

In a metal-insulator-semiconductor (MIS) structure with a finite lateral extent, a quasi-two-dimensional electron system (2DES) will develop in a potential well on the metal side or the semiconductor side, depending on the polarity of the bias, and strong Coulombic repulsion is expected in the local area around the edge of 2DES [8]. Due to the strong Coulombic repulsion, the potential energy of the electrons is enhanced, and the equivalent work function at the edge of 2DES becomes very small. In other words, the vacuum barrier height at the cathode is very low, similar to the negative electron affinity effect. Electrons around the edge of 2DES can travel over the barrier at room temperature following the thermal emission regime and governed by space charge limitation (SCL). With an increase in bias, the virtual cathode of the space charge will locate on the cathode, and the electron emission will be subjected to the Schottky emission regime. By further increasing the positive bias, the width of the barrier becomes narrow enough for electrons to tunnel through, and the electron emission will then be subjected to the Fowler-Nordheim (F-N) regime. These three different regimes were observed when testing a MIS structure with a void channel in our experimental work (see Supplementary Fig. 1). In this study, in considering the structure and bias we defined, we primarily focused on the performance of the device that works in the F-N regime. When working in field emission regime, such a device is more suitable for applications in harsh operating conditions such as high temperature and irradiated environments. Also, it provides higher output power than in the other two regimes.

The structure of the device we proposed was vertically aligned with a multilayer combination of dielectric layers and metal layers as depicted in Fig. 1. The materials of the cathode/gate/anode were aluminum/ITO/p-type silicon (resistivity = 10 Ωm, (100)-oriented). The material of dielectric layers was silicon nitride (Si_3N_4). When certain positive voltages were exerted on the gate and anode, the 2DES was formed at the aluminum side of the interface of Si_3N_4 and Al (with a width of <1 nm) [8] where electrons are easily emitted from. The emitted electrons travelled ballistically through the vacuum channel and were finally captured by the anode. The channel current was simultaneously controlled by the gate and anode voltage. The current component of electrons directly emitted from the gate (ITO) was negligible compared to the current emitted from the cathode due to the easier 2DES formation on the cathode than on the gate (i.e., the dielectric thickness t_{CG} is much thinner than t_{GA}). Tunneling of the current component directly through the gate dielectric layer [15] and collected by the gate were not found in our experimental results; we did not witness the F-N regime while testing the MOS structure without a vacuum channel in the bias range we used (see Supplementary Fig. 2). Other structural parameters we used in the simulation work are listed as follows: vacuum channel radius r was investigated varying from 1 nm to 100 nm; Al/ITO/t_{GA}/p-type Si were set to 20 nm/5 nm/30 nm/10 nm; and the gate dielectric thickness t_{CG} was set to 10 nm, 15 nm, and 20 nm respectively for comparison.

3. Simulation technique

To investigate the vertically aligned vacuum transistor, a 3-D electrostatic and particle solver program based on finite integration technique (FIT) was adopted. The electrostatic field distribution was automatically calculated under given biasing conditions. Within an intense electric field, electrons tunnel though the energy barrier on the cathode surface and are then emitted into the vacuum. The field emission process was simulated via the Fowler–Nordheim equation (F–N) [16]. With the solved electrostatic field, particles trajectories were tracked. The current of each component was obtained by taking note of all the collision events. Iteration algorithms were implemented until all the space charge effect [17–19] violations were solved. More details on the simulation technique can be found in our previous work [20,21].

The F-N equation for the field emission process is expressed as

$$J = \frac{AE^2}{\phi}\exp\left(\frac{-B\phi^{3/2}}{E}\theta(y)\right) \quad (1)$$

where A and B are fitting parameters, ϕ is the equivalent work function [22,23] of the emission surface, and $\theta(y)$ is the Nordheim function. E is the normal component of the electric field at the emitter surface and given by $(V_g + V_a/\mu)/d$ [24,25]; μ is given as [24]

$$\mu = -\frac{\partial V_a}{\partial V_g}\Big|_{I_a=constant} \quad (2)$$

As noted above, the 2DES was confined in a potential well with a width of less than 1 nm, so the emission area was also less than 1 nm in width (here we set it as 1 nm for the sake of simplicity) and located at the edge of the 2DES where strong Coulombic repulsion was expected. Due to the Coulombic repulsion, the equivalent work function of the emission surface was much lower. The deviation of the work function theoretical can be calibrated with experimental

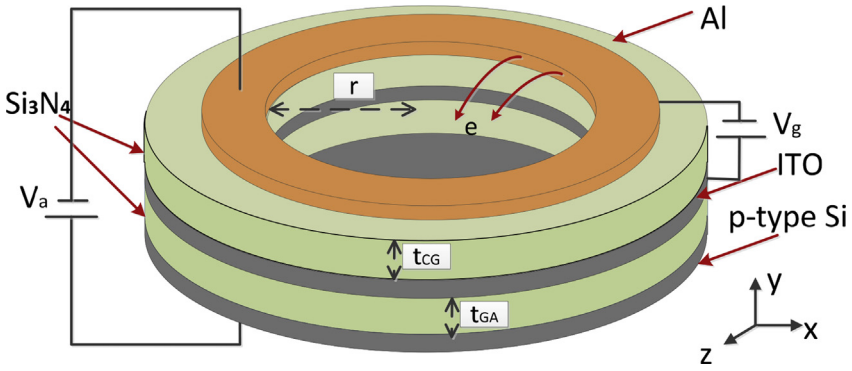

Fig. 1. Schematic of the proposed vacuum channel transistor.