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Analysis design of area efficient segmentation digital to analog converter for ultra-low power successive approximation analog to digital converter

Iffa Sharuddin*, L. Lee, Zubaida Yusof

Faculty of Engineering, Multimedia University, Persiaran Multimedia, 63100 Cyberjaya, Selangor, Malaysia

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ABSTRACT

This article presents analysis design of area efficient segmentation analog to digital power successive approximation analog to digital converter. A 10-bit 10-kS/s successive approximation analog-to-digital converter (SAR ADC) is designed by using 0.18 μm CMOS technology. The SAR ADC has been designed by using the segmentation technique which employed two different digital to analog converter (DAC) architectures. The proposed DAC design shows significant reduction in terms of area and better linearity. The overall speed of the ADC has greatly reduced due to lower switching activity. The supply voltage used is 1.5 V. At 10-kS/s sampling rates, the total power consumption of the whole SAR ADC is equaled to 7 nW while for DAC alone is 2.7 nW.

1. Introduction

The need for low power consumption circuit is becoming more important in the market today especially in the analog design. This is due to the increasing demand in battery-powered electronic devices which require lifelong battery. To have low power consumption devices, the circuit needs to operate in low power supply. This is a challenge for mixed signal systems. Successive Approximation Analog to Digital Converter (SAR ADC) is a popular approach nowadays due to its simplicity and ultra-low power consumption.

The conventional SAR ADC consists of sample and hold (S/H) circuit, comparator, SAR register and digital to analog converter (DAC). The conversion process is performed in three consecutive modes of sample, hold and charge redistribution mode. Sample and hold modes are normally for S/H circuit operation. During charge redistribution modes, the DAC output voltage is compared successively with the sampled input voltage one bit at a time through N clock cycle. This method is called the binary search algorithm which is the most popular method in ADCs due to lower switching activity. Most of the recent SAR ADC architectures do not require S/H circuit anymore since it can be done by the capacitor array itself. The capacitor array will act as both DAC and S/H functions. Hence, the comparator will perform the comparison with the reference sampled input voltage produced by the DAC beforehand. However, it required extra switching activities at the top and bottom plate of the capacitor array in which it will generate more power as compared with the use of external S/H circuit. The block diagram of proposed SAR ADC is shown in Fig. 1. It uses separate S/H circuit to perform the binary search method.

This proposed ADC is well suitable for biomedical application where the input signal frequency is usually less than 40 KHz [1]. An implant device in human body is required to last for over a decade or more by consuming only nanowatts of power consumption. The signal acquired from the human body by biosensor such as electrocardiography (ECG) is very weak, so the moderate speed ADC is preferred in any biomedical systems [2]. The sampling speed in biomedical application can be relaxed and usually in the range of 1-kS/s to 200-kS/s. In this paper, a 10-kS/s sampling frequency is proposed with the 10-bit resolution of ADC which suits biomedical application.

2. SAR ADC operation

Fig. 2 shows the timing clock diagram for the whole SAR ADC operation. There are two external clock used in this design which are ADC clock (CLK_{ADC}) and sample and hold clock ($CLK_{S/H}$). The SAR logic circuit will generate control signal for all switches for MSB bit and LSB bit to generate the reference voltage level to execute the binary search algorithm through DAC circuit.

The operation of the binary search algorithm for 10-bit ADC is shown in Fig. 3. For 10-bits ADC, it takes about 11 clock cycle to complete the binary search. The first clock cycle is reserved for

* Corresponding author.

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sampling phase and reset phase of all SAR logic register D[0:9]. The rest of the clock cycle will perform the comparison and decide the final digital output of the sampled input voltage.

The S/H circuit has two operation modes which are sample and hold phases. When $CLK_{S/H}$ is high, it enters the sampling phase and sampled the input signal, *Vin*. At the same time, the entire capacitor array is connected to the ground as all register will be set to zero. Hence, no voltage is present at the DAC output node. During holding phase, the sampled input voltage, V_{samp} does not change its value as it will be used for the comparison process. At the second clock cycle, SAR register starts to operate and produce binary word 1000000000 which in turns set the MSB bit to one. This indicates the starting point of the comparison process. Once the DAC received the binary word, it will produce the reference voltage, V_{DAC} and the comparator will compare the V_{DAC} with V_{samp}. The comparator will produce logic one and zero depending on the comparison result as describe in Eq. (1).

$$V_{CMP} = \begin{cases} 0, V_{DAC} > V_{samp} \\ 1, V_{DAC} < V_{samp} \end{cases} \quad (1)$$

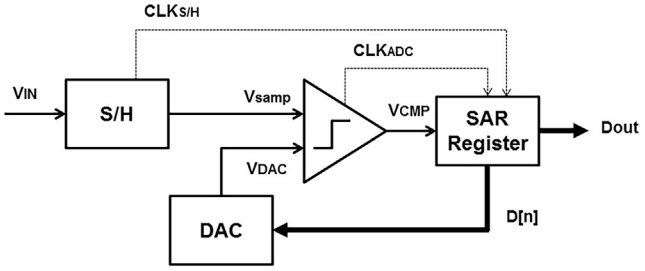

Fig. 1. Block Diagram of a SAR ADC architecture.

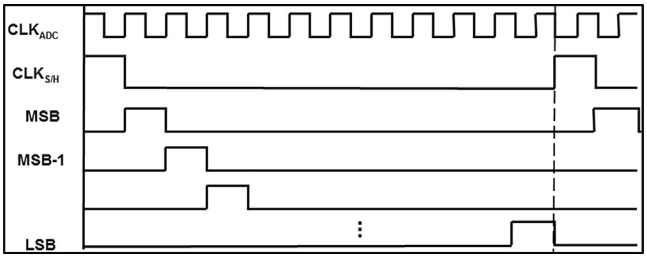

Fig. 2. Timing for SAR ADC operation.

The value of the reference voltage V_{DAC} will be updated to be closer to the input signal based on the comparison result. The MSB bit will remain high if V_{CMP} produce 1 and likewise if it changed to 0. Once the first MSB is obtained, the next MSB bit will be set high to determine the next digital value. This process will continue until the last bit is obtained to form 10-bit codeword.

3. The proposed 10-bit SAR ADC

The SAR ADC architecture presented is based on charge redistribution technique with separate sample and hold circuit. The DAC will operate as an individual block. This will reduce the DAC switching activities in the capacitor array and could produce less error due to complex switching activities. The switching network should be made simple to ease the overall ADC operation for high resolution circuit design. To further reduce the total capacitance of the capacitor array, the segmentation technique has been used in the DAC architecture. The SAR ADC is realized by using single ended input signal.

The drawbacks of the binary-weighted capacitor (BWC) array are large area and high power consumption [3]. The total capacitor value increases exponentially with the number of bits and the minimum value of unit-capacitor is restricted by kT/C noise. Add on to that, the settling time of DAC increases in the binary weighted capacitor.

3.1. Digital to analog converter

BWC DAC is the most popular approach to implement DAC block. However, it contained large numbers of capacitor to realize a high resolution ADC. The capacitor value is distributed under the condition of voltage ratios ranging from $\frac{1}{2}$ to $\frac{1}{2^N}$ at the DAC output terminal. Basically, it starts with C, $2C$, $4C$, $8C$, $16C$ until $2^{N-1}C$ where N denotes the resolution of the ADC. The BWC DAC needs to charge and discharge each capacitor according to the comparison process and MSB bit has the highest capacitor value which correspond to $2^{N-1}C$. The drawback of this process is that it consumed lots of power during the switching process. This distribution is not suitable for high resolution ADC because the value of capacitor increases exponentially with the number of resolution. Splitting method in [4] is proposed to overcome this problem. Other than that, segmentation technique has been proposed [5,6]. Basically, segmented DAC composed of MSB and LSB segment which correspond to different DAC architecture which is connected through a

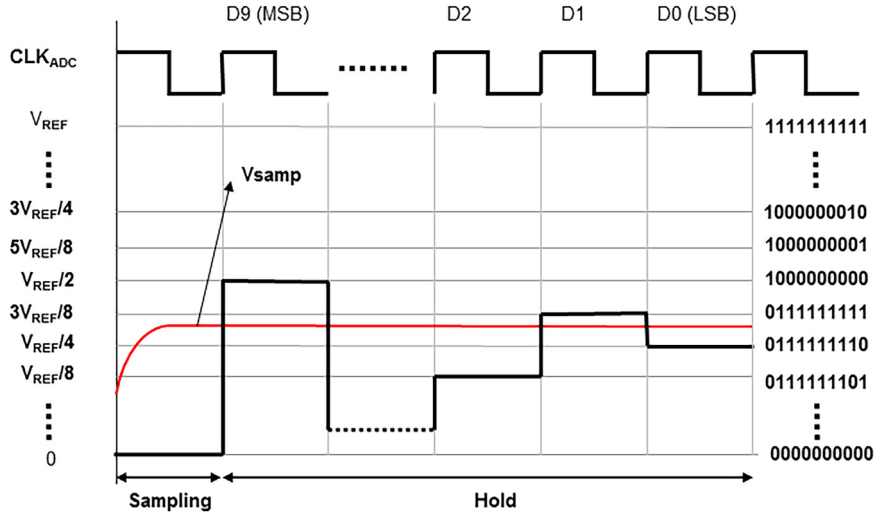

Fig. 3. Binary search operation.