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## Infrared spectroscopic analysis of reactively formed La-silicate interface layer at $\text{La}_2\text{O}_3/\text{Si}$ substrates<sup>☆</sup>

K. Kakushima<sup>\*</sup>, T. Seki, H. Wakabayashi, K. Tsutsui, H. Iwai

School of Engineering, Tokyo Institute of Technology, Yokohama 226-8502, Japan

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### ABSTRACT

Infrared spectroscopic analyses of reactively formed La-silicate gate dielectrics between  $\text{La}_2\text{O}_3$  and Si substrates are conducted with the attenuated total reflection configuration. The formation of a La-silicate interface layer at the surface of Si(100) has been confirmed with an annealing temperature of 300 °C and the layer has grown with increasing the annealing temperature. The strain in the  $\text{SiO}_4$  tetrahedral network in the La-silicate interface layer, measured from longitudinal optical phonon vibration, showed relaxation when annealed at over 600 °C, suggesting a decrease in glass transition temperature owing to the presence of La atoms in the network. A strong correlation between the relaxation and the interface state density has been confirmed. The same relaxation trend with annealing temperature has been confirmed for Si(110) and (111) surfaces as well.

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### 1. Introduction

The progress in  $\text{HfO}_2$ -based high-k gate dielectrics has enabled aggressive scaling of silicon-based metal-oxide-semiconductor (MOS) devices [1]. The films have been continuously utilized in scaled devices including FinFETs, and the immunity against the short-channel effect has been greatly improved [2]. The deposition of  $\text{HfO}_2$  films commonly commences with surface treatments of the channel region to improve the adhesion of  $\text{HfO}_2$  layers, resulting in a  $\text{SiO}_2$ -based interface layer (IL) [3]. The IL also improves reliability by reducing interface state density ( $D_{it}$ ). However, fixed charges ( $Q_{fix}$ ) and traps located in the  $\text{HfO}_2$  layer and IL produce shifts in flatband voltage ( $V_{fb}$ ), and the slow state response to the traps increases flicker noise in drain current [4,5]. In terms of scaling, the presence of the IL poses difficulty in the further reduction in equivalent oxide thickness (EOT).

On the other hand, La-silicate gate dielectrics have shown fairly good interface properties without the presence of a  $\text{SiO}_2$ -based IL [6]. La-silicate is formed as a result of the reaction between  $\text{La}_2\text{O}_3$  layers and Si channels in two steps: the formation of a  $\text{SiO}_2$  layer at the interface, followed by the dissolution of La atoms into the  $\text{SiO}_2$

layer. By selecting a proper thermal treatment with oxygen-partial-pressure control, one can well control the thickness and composition of the La-silicate layer. [7]. Owing to the elimination of the  $\text{SiO}_2$ -based IL, down-scaling to 0.6 nm has been demonstrated with excellent gate leakage current suppression. One of the prominent features of the reaction is that there is no dependence on crystallographic orientation, which is advantageous for FinFET and future Si nanowire (SNW) FETs [8].

A typical method of obtaining low  $D_{it}$  with La-silicate gate dielectrics is to anneal the gate stack at over 800 °C, where a monotonic reduction in  $D_{it}$  is observed up to this temperature. The physical origin of the required annealing temperature is not clear, but, it should reflect the bonding configuration of the La-silicate film. La-silicates were reported to have three-dimensional silicon tetrahedron ( $\text{SiO}_4$ ) networks modified with La atoms [9]. As a result, the bonding nature is more covalent than that of other polycrystalline high-k films that have a more ionic nature, so that the oxygen ionic conductivity becomes extremely low [10]. In addition, as La-silicates are in the amorphous state under typical semiconductor processes, it can be speculated that the bonding configuration in the La-silicates may influence  $D_{it}$ . Indeed, for  $\text{SiO}_2/\text{Si}$  sub. a strong correlation between the strain in the  $\text{SiO}_2$  layer and  $D_{it}$  has been reported [11].

To elucidate the strain in the thin dielectric films, Fourier transform infrared spectroscopy (FTIR) with the attenuated total reflection (ATR) configuration has been an effective tool [12]. By combining it with wet etching process of the surface of the  $\text{SiO}_2$

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<sup>\*</sup> Corresponding author.

E-mail address: [kakushima.k.aa@m.titech.ac.jp](mailto:kakushima.k.aa@m.titech.ac.jp) (K. Kakushima).

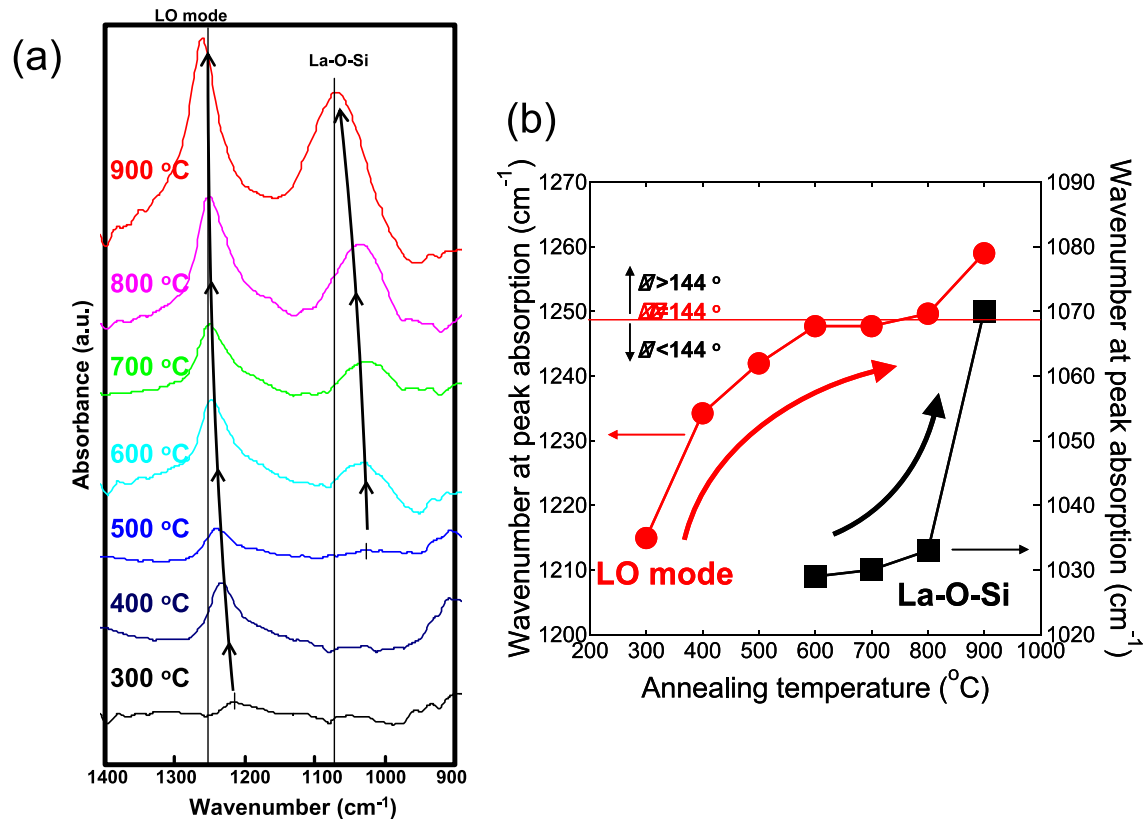


Fig. 1. (a) IR spectra of the samples after annealing. (b) The absorption peak wavenumber of the Si-O-Si LO phonon and La-O-Si modes show a redshift with increasing annealing temperature.

layer, the presence of strain in the  $\text{SiO}_4$  tetrahedral networks within the thin  $\text{SiO}_2$  layer adjacent to the interface has been characterized [13]. In this work, the strain in the networks of La-silicate layers formed under different annealing conditions was characterized by FTIR-ATR, and the correlation between the strain and the  $D_{it}$  was investigated using Si substrates with different crystallographic orientations.

### 1.1. Sample preparation and measurements

The Si wafers used in this study were n-type Si (100), (110), and (111), with the same doping density of  $3 \times 10^{15} \text{ cm}^{-3}$ . After chemical cleaning followed by HF dipping, 4-nm-thick  $\text{La}_2\text{O}_3$  dielectrics were deposited by e-beam evaporation at a deposition rate of 0.2 nm/min and a pressure of  $10^{-6}$  Pa. The substrate temperature during the depositions was maintained at 300 °C. Then, a 10-nm-thick W or TiN metal was deposited *in situ* by RF sputtering. The samples were subjected to post metallization annealing (PMA) by rapid thermal annealing (RTA) in forming gas (FG) ( $\text{N}_2:\text{H}_2 = 97:3\%$ ) ambient with various annealing temperatures and durations. Infrared (IR) absorbance measurements were performed by the ATR method with a Ge prism ( $65^\circ$ ) through the metal layer. As the thickness of the W layer is set to 10 nm, the absorption spectra of the reactively formed La-silicate layers can be detected [14]. The resolution was set to  $8 \text{ cm}^{-1}$  and the area for measurement was set to  $7 \text{ mm}^2$ . To directly observe the interface reaction and the composition, hard x-ray photoelectron spectroscopy (HXPES) measurements at SPring-8 BL47XU were carried out for some samples with 10-nm-thick W layers. For  $D_{it}$  extraction, MOS capacitors with a  $\text{La}_2\text{O}_3$  thickness of 3 nm were fabricated. The detailed fabrication process for MOS capacitors is described in

Ref. [15].

## 2. Results and discussion

IR absorption spectra obtained for various annealing temperatures are shown in Fig. 1(a). The duration of annealing was fixed to 30 min. In this figure, two distinct peaks are observed: one ranging from 1215 to  $1250 \text{ cm}^{-1}$  and the other near  $1050 \text{ cm}^{-1}$ . The peaks observed from 1215 to  $1250 \text{ cm}^{-1}$  are for the longitudinal-optical (LO) vibrational modes of bridging O atoms in the  $\text{SiO}_4$  tetrahedral networks and strongly reflect the strain in the film. The peaks

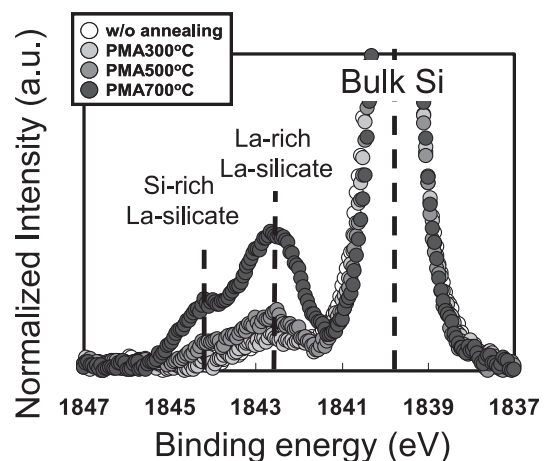


Fig. 2. Si 1s spectra of W/ $\text{La}_2\text{O}_3$ /nSi structure without annealing, and with annealing at 300, 500, and 700 °C.

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