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A curvature-compensated CMOS bandgap with negative feedback technique

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ABSTRACT

This paper propose a novel high-order curvature-corrected CMOS bandgap reference (BGR) utilizing the negative feedback structure. The innovative negative feedback bandgap core not only compensates the exponential nonlinearity of VBE but also improves the power supply rejection ratio (PSRR) and line regulation. The proposed BGR is analyzed and implemented in 0.35-μm CMOS process. Experimental results of the BGR indicate that a minimum temperature coefficient (TC) of 13 ppm/°C @ − 40 °C to 180 °C, a PSRR of − 64 dB @ 100 Hz, and the 5.2 uV/V line regulation (LNR) from 3 V to 3.6 V supply voltage at room temperature. The active area of the presented BGR is 133 μm × 300 μm.

1. Introduction

Precision voltage reference plays an important role in ADC, DAC and LDO circuits. The temperature coefficient and power supply rejection ratio are two key factors defining the performance of the reference, and a low TC and high PSRR reference are highly preferred.

With regards to the non-linearity of emitter-base voltage of bipolar junction transistor (BJT), the TC of the first-order bandgap reference is limited between 20 and 100 ppm/°C [1,2]. In order to improve temperature performance, some compensation techniques have been developed through the addition of a second-order or high-order proportional to absolute temperature (PTAT) term to the output reference voltage, which is denoted as curvature-corrected bandgap references [3].

In theory, $T\ln(T)$ correction is the best way to compensate the nonlinearity of V_{BE} [1]. However, it is quite difficult to realize such advanced mathematical function with high accuracy in circuits. Most of the curvature-corrected BGRs use a proximate way to compensate this nonlinear component. A piecewise nonlinear squared-PTAT current flowing through MOSFET is added to the first-order BGR to compensate the nonlinear V_{BE} in high temperature [4]. In either case, we could use PTAT and CTAT currents to implement the second-order curvature-compensation [5]. Instead of second-order compensation technique, a class of exponential and logarithmic curvature compensation is used to decrease the temperature drift in whole temperature range and achieves 5 ppm/°C [1]. High-order curvature-compensation also can be achieved by utilizing a variable gain current mirror to realize exponential compensation [6]. In BiCMOS, a diode connected bipolar transistor is used to generate a current proportional to the nonlinear $T\ln(T)$ and subtracted it from the current in core circuit [11].

In order to improve PSRR, a self-biased symmetrically matched current–voltage mirror is presented to enhance the PSRR up to − 50 dB with 0.35 μm CMOS process [7]. Two negative feedback loops to achieve − 80 dB PSRR performance with TSMC 0.35 μm CMOS process, which are the pre-regulator of line voltage and a negative feedback loop in the bandgap core [8]. The high PSRR strategies also include bandgap circuit operates from an internal regulated supply VREG made with a high gain feedback loop [9] or bandgap core is supplied from a current source independent from supply [10].

In this paper, we proposed new circuit architecture to improve a BGR's TC as well as the PSRR. The proposed circuit incorporates a negative feedback in the first-order voltage reference core architecture for the curvature corrected compensation and high PSRR. The proposed curvature compensation principle only requires an additional MOSFET. Curvature compensation is achieved by subtracting the non-linear current from Q2 BJT, while the solution presented in [11] use the dioded-connect BJT and subtracting the current from both Q1 and Q2. Till now, no bandgap voltage reference based on this proposed negative feedback technique has been proposed in any paper.

This paper starts with a brief analysis on the principle of classic bandgap references in Section 2. The proposed high-order curvature-corrected CMOS bandgap with negative feedback technique is

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introduced in Section 3. Simulated and measurement results, performance comparison with some other reported bandgap references are presented in Section 4. Finally, the conclusion is given in Section 5.

2. Principle of the first-order BGR

In CMOS technology, parasitic BJTs formed in n-well or p-well are commonly used to implement the bandgap voltage reference. Fig. 1 shows the traditional first-order CMOS BGR circuit [6]. The feedback loop constructed by P_1-P_2 and N_1-N_2 forces the voltage $V_A=V_B$, the current of R_1 is

$$I=\frac{V_{EB2}-V_{EB1}}{R_1}=\frac{V_T\ \ln(M(N+1))}{R_1} \tag{1}$$

where V_{BE} means the emitter-base voltage of bipolar junction transistor, V_T represents the thermal voltage and M is the emitter area ratio of Q_1 and Q_2. N means that P_3 mirrors N times current of P_1 or P_2, so the output voltage is

$$V_{REF}=V_{EB2}+N\frac{R_2}{R_1}\cdot V_T\ \ln(M(N+1)) \tag{2}$$

The relationship between temperature and emitter-base voltage of PNP BJTs, which are biased in forward active region, can be expressed as [3]

$$V_{EB}=V_{G0}-\frac{V_{G0}-V_{EB}(T_0)}{T_0}T-(\eta-m)\frac{kT}{q}\ln\left(\frac{T}{T_0}\right) \tag{3}$$

where V_{G0} is the bandgap voltage of silicon extrapolated at 0 K, T_0 is the reference temperature, k is Boltzmann's constant, η is a temperature constant depending on the technology, and m is the order of the temperature. At room temperature $\partial V_{EB2}/\partial T\approx-1.5$ mV/°K and $\partial V_T/\partial T=k/q\approx 0.087$ mV/°K [12], q is electronic charge.

In Eq. (3), the second term $\frac{V_{G0}-V_{EB}(T_0)}{T_0}T$, and the third term $(\eta-m)\frac{kT}{q}\ln\left(\frac{T}{T_0}\right)$ are the linear and nonlinear temperature-dependent factors of V_{BE}. The classical first-order BGR circuit only compensates for the linear term by setting resistance values of R1 and R2 of Eq. (2) to cancel the 2nd term. In order to further improve the TC performance, high-order curvature-corrected compensation should be studied and developed.

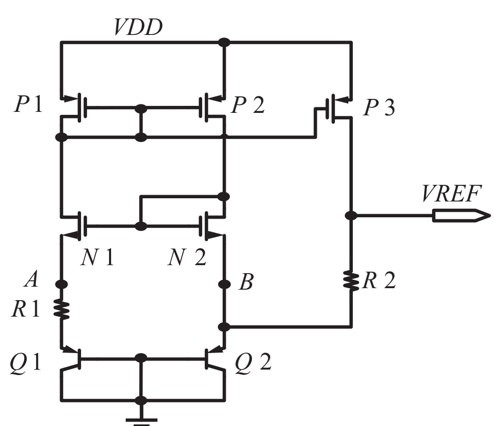

Fig. 1. The classic bandgap reference structure.

3. Proposed curvature-corrected CMOS BGR with negative feedback

In addition to the quadratic, exponential, and piecewise compensation schemes, we propose an innovative negative feedback based compensation by adding a correction current to the PTAT collector current. The proposed bandgap reference circuit is shown in Fig. 2, and the deviations from the traditional design are highlighted. The BGR consists of voltage regulation, reference voltage generation, PSRR enhancement and start-up block.

3.1. Temperature coefficient analysis

As shown in Fig. 2, the negative feedback loop constructed by P_{1-2}, N_{1-2} is justifiably called a self-biased current–voltage mirror (CVM) [7]. P_{1-2} serve as a current mirror, forcing $I_{N1}=I_{N2}=I$, and N_{1-2} with their gates being connected together and with the same drain currents, serve as a voltage mirror, forcing $V_A=V_B$. The current of R_1 can be expressed by

$$I\cdot R_1=V_{EB2}-V_{EB1} \tag{4}$$

Assuming that P_3 mirrors N times current of P_1, and the emitter area ratio of Q_1 and Q_2 is M, we obtain the following equations:

$$\begin{cases} V_{EB1}=V_T\cdot\ \ln\left(\frac{I}{MI_S}\right) \\ V_{EB2}=V_T\cdot\ \ln\left(\frac{(N+1)I-I_{N3}}{I_S}\right) \end{cases} \tag{5}$$

Substituting (5) into (4) gives

$$I\cdot R_1=V_T\cdot\ \ln\left(\frac{(N+1)I-I_{N3}}{I_S}\right)-V_T\cdot\ \ln\left(\frac{I}{MI_S}\right) \tag{6}$$

The current I_{N3} can be described as $K(V_{REF}-V_{THN})^2$, where K represents $(\mu C_{ox}W/L)_{N3}/2$ and V_{THN} is the threshold voltage. The

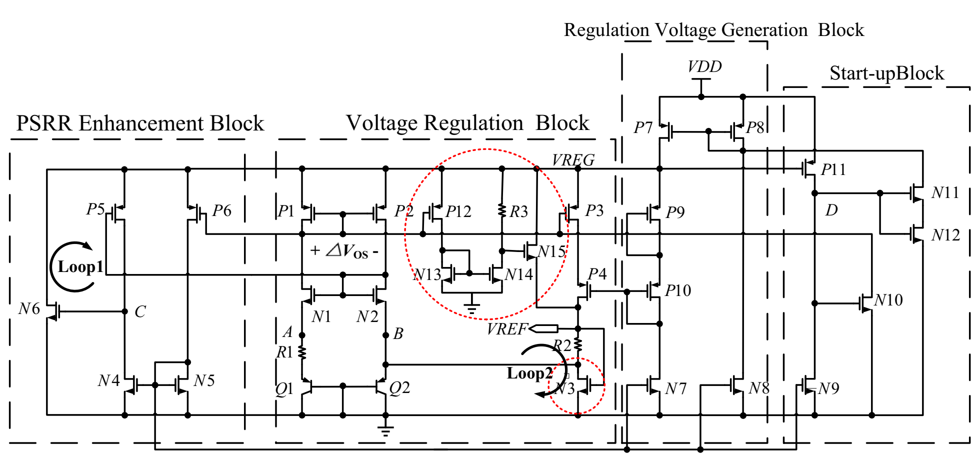

Fig. 2. Schematic of the proposed BGR.