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Low voltage high performance bulk driven quasi-floating gate based self-biased cascode current mirror

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ABSTRACT

A low voltage high performance self-biased cascode current mirror in terms of output resistance and bandwidth is proposed in this paper. The proposed current mirror enhances the output resistance in range of mega ohms and also shows a significant improvement in bandwidth compared to prior arts. The current mirror is designed using bulk-driven technique which helps it to operate at very low supply voltage of ±0.2 V. To achieve high output resistance, the proposed current mirror uses the super cascode stage at its output. Furthermore, an external capacitor is used which accounts for increasing the bandwidth. Small-signal analysis carried proves the improvement achieved by proposed architecture. The current mirror operates well for wide input current range from 0 to 200 μA with good linearity and shows the bandwidth of 415 MHz. The observed input and output resistance is 300 Ω and 212 MΩ respectively. Further, the THD and mismatch analysis is carried to prove the robustness of proposed current mirror. The complete analysis of proposed current mirror is shown using HSpice simulations on UMC 0.18 μm technology.

1. Introduction

The increasing demand of smart efficient portable medical and electronic devices with longer battery life has forced the industry to use reliable techniques for designing analog and mixed-signal circuits at low voltage in deep sub-micron technology [1]. Following a conventional gate driven (GD) technique for circuit realization becomes no more effective at sub-volt supply due to threshold voltage of MOS transistor (MOST). Moreover, reduced voltage supply strongly affects the performance of analog circuits as compared to digital. Various non-conventional design techniques have been proposed in literature which favours the low voltage and help in design of efficient low power circuits. Some of well known techniques frequently used are subthreshold [2], level shifter [3], bulk-driven (BD) [4–6], floating gate (FG) [7–9], quasi-floating gate (QFG) [10,11], and bulk-driven floating/quasi-floating gate (BDFG/BDQFG) [12]. Each of the aforementioned technique has its importance in specific applications. Among the stated techniques the BDQFG has gained considerable interest due to significant improvement in transconductance and so the transition frequency over simple BD MOST. The BD technique suits low power circuit design due to its simple structure and threshold free input signal path as the applied DC potential at gate creates the channel for MOST to turn ON. In BD MOST the bulk-to-source voltage controls the drain current. Based on BD, the very first circuit was reported in design of differential pair [13]. The only drawback with BD technique was its low value body transconductance (g_{mb}) and transition frequency (f_T) [14] which got resolved using the technique named BDFG/BDQFG. The BDFG/BDQFG technique results in effective transconductance as a sum of body transconductance and scaled gate transconductance (i.e. transconductance of FG/QFG MOSFET) respectively. The QFG are wideband ac coupled circuits which blocks the dc offset voltage of input without degrading the frequency response [15]. Moreover, the capacitor divider network at QFG node offers better linearity and suits low voltage operation by scaling down the threshold voltage. The bio-signals being small in amplitude and low frequency range (KHz) suits BDFG/BDQFG approach for signal processing [16]. Few latest articles using BDQFG technique can be observed in realisation tunable transconductor [17], differential difference current conveyor [18], differential difference amplifier [19], rectifier [20], transconductor based filter [21] etc.

Current mirror is the basic building block of voltage and current mode circuits. The primary function of current mirror is to copy the input current at its high impedance output node. The commonly used applications of current mirror are level shifting, biasing, active loading etc [22], and also in filter realization [23].

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Thus design of high performance current mirror is the key requirement of analog circuits. The high performance here is defined in terms of wide current driving capability, high linearity, low input and high output impedances, and high bandwidth. In deep submicron technology, the simple current mirror does not fulfil the required performance. The increased output conductance due to short channel MOS device results in poor matching of input-output current. In view to this, various topologies have been proposed in literature to achieve the ideal characteristic of current mirror. The very common architecture used as replacement of simple two transistor based current mirror is the cascode current mirror (CCM) [22]. The CCM offers high output impedance and suits high performance applications like in design of second generation current conveyors, op-amps, LNA etc. The major drawback with such current mirror was the overdrive voltage required by output transistors which lowers the output swing. Later the CCM was then modified by using a resistor R at its input and named as self-biased high swing cascode current mirror (SHCCM). Being simple in architecture this current mirror gained potential interest. Further, this current mirror was realized using BD technique in [24] which when compared with conventional architecture realized using GD technique showed improvement not only in terms of low voltage operation but also results in improved performance parameters. Later in [25] the BD SHCCM architecture got modified using BDQFG technique where a significant improvement in input resistance and bandwidth was observed. Though BDQFG SHCCM proved its performance better in terms on input resistance and bandwidth but yet the architecture lags in terms of high output resistance. Other articles reporting high performance low power current mirror in literature based on BD can be found in [26], based on QFG can be found in [27–29]. Though QFG based current mirror circuits have proven their advantage in terms of low voltage operation but experiences the problem of DC convergence with the available Spice simulators in the market. For DC simulations, the QFG circuits require an additional arrangement for example the commonly used approach is putting a very high value resistor in parallel to capacitors. But the issue got resolved with the advent of BDQFG technique. Under DC condition, circuits based on BDQFG shows BD type behavior whereas for AC the architecture results in combined characteristic of BD and QFG. This paper presents a high output resistance and high bandwidth SHCCM using BDQFG. The proposed current mirror architecture is divided in three parts where the first proposed current mirror is realized using BD (Proposed-I) and then followed by BDFG (Proposed-II) and finally BDQFG (Proposed-III) so as to show the importance of each technique over other.

The paper is divided in five sections. Section 2 details the architecture of BDQFG MOST followed by proposed current mirrors in Section 3. Further, the small-signal analysis of proposed current mirror is also shown in Section 3. The simulation results are discussed in Section 4 followed by conclusion in Section 5.

2. BDFG and BDQFG MOSFET

The BDFG/BDQFG MOST is similar to that of BD MOST, except the difference lies in gate-node potential. In BDFG/BDQFG instead of applying gate to a fixed DC potential, it is configured in floating/quasi-floating state. The schematic of an N-channel BDFG and BDQFG MOST along with its parasitic capacitances is shown in Fig. 1(a) and (b) respectively.

In Fig. 1(a), the gate of MOST MN is converted in floating state using input capcitor (C_{in}) and its other end connected to bulk so as to make it bulk controlled device and the architecture results as BDFG MOST. A biasing capacitor (C_{bias}) is also used at gate of MN to keep BDFG MOST in saturation mode. In the same way in Fig. 1(b), BDQFG MOST is formed with only difference is that the gate of MOST is converted from floating state to quasi-floating state by weakly connecting it to supply rail VDD via a high value resistor (R_{large}). The resistance R_{large} is realized using minimum-size diode-connected P-channel MOST MP in the cut-off region consuming negligible extra area [30]. Moreover, due to absence of C_{bias}, the BDQFG MOST results in improved gain-bandwidth product. The use of R_{large} causes MN MOST floating for low frequency signals and do not affect the ac operation. The effective gate potential of BDQFG in s-domain is given as

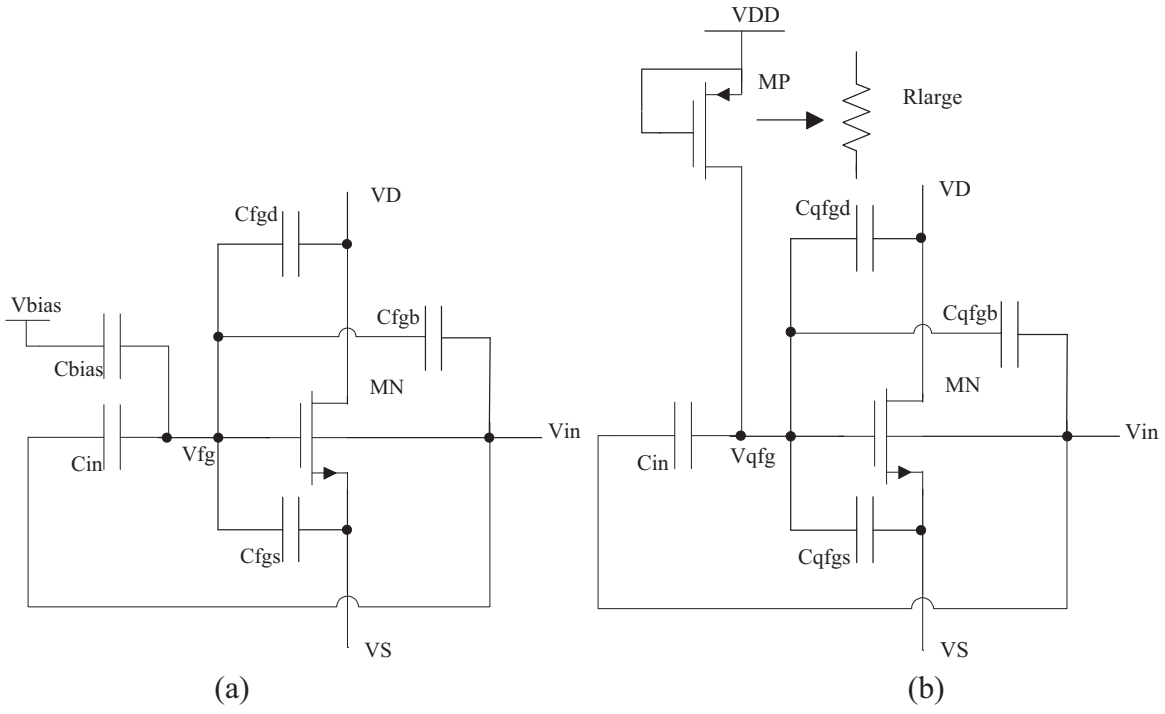

Fig. 1. Equivalent circuit of N-type: (a) BDFG and (b) BDQFG MOST.