Microelectronics Journal 51 (2016) 46–57

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

Statistical yield improvement under process variations of multi-valued memristor-based memories

Hassan Mostafa [a,b,*], Yehea Ismail [b]

[a] Electronics and Communications Engineering Department, Cairo University, Egypt
[b] Center for Nanoelectronics and Devices, Zewail City of Science and Technology, AUC, Egypt

ARTICLE INFO

Article history:
Received 6 September 2015
Received in revised form
10 January 2016
Accepted 11 February 2016
Available online 5 March 2016

Keywords:
Memristor-based memory
Process variation
Statistical yield improvement
Multi-valued memory

ABSTRACT

Memristor, the missing fourth element predicted by L. Chua, has recently been in the research focus since HP Lab reported the first TiO_2 thin film memristor realization. The nano-scale geometry size of the memristor makes it difficult to control its dimensions due to the process variation incurred in the fabrication process. This process variation results in yield degradation in the memristor-based memories. This yield degradation is more severe when the memristor device is used as a multi-valued memory element. In this paper, the impact of the process variation on the memristor-based memory yield is investigated for the 1-bit, 2-bit, and n-bit memristor memory element. In addition, two approaches are proposed to improve the memory yield. Therefore, the main objective of this work is to introduce a statistical yield simulation flow to calculate the memory statistical yield under process variations and investigate the effect of different design knobs on this statistical yield regardless of the memristor models and the process variation models used. Simulation results reveal that for 1-bit memristor-based memories, the nominal write voltage should be increased by 30% and the nominal threshold value (i.e., the midway memristance value between the memristor ON resistance and the memristor OFF resistance) should be increased by 65% to achieve the maximum yield. Finally, the paper lists the minimum memristor size that should be used to achieve a 99.9% memory yield for n-bit memories. These results show how the process variation imposes limitations on the minimum memristor device size when multi-valued memories are to be designed.

1. Introduction

In 1971, the father of the memristor, Chua, predicted that there was a missing fourth passive circuit element and denoted it by memristor [1]. The dream of having a real practical implementation of the memristor was on hold from 1971 to 2008. In 2008, this dream has come true when Williams introduced a two-terminal Titanium dioxide (TiO_2) nano-scale device that followed the memristive characteristics defined by Chua in 1971[2–4]. As portrayed in Fig. 1, Chua predicted that there was a missing relationship between ϕ and q, and he denoted this missing fourth passive element by Memristance (M) [1]. Typically, a linear memristor acts as a resistor. However, if the ϕ-q relationship is nonlinear, the device behavior is different from that of a resistor. Charge-controlled memristor characteristics are investigated in more details in [5]. According to [4], the memristor maintains its memristance value even if the bias voltage is removed. This unique characteristic makes the memristor a very promising candidate to be used as a non-volatile memory element.

Recently, the memristor has gained significant attention on the device manufacturing, Computer-Aided-Design (CAD), circuit, and architecture levels [6–9,5,10–14]. As stated by Williams from HP, the memristor is the potential candidate to replace the CMOS transistor in the near future thanks to its smaller area and power consumption [13,14].

The demand for high density memory structures has motivated the memory designers to focus on the next generation universal memories that is anticipated to replace the conventional memory technologies such as Dynamic Random Access Memories (DRAMs) and Static Random Access Memories (SRAMs). The nonvolatile advantage of the memristor-based memories makes this technology one of the promising candidates for the next generation memory technology. Memristor-based memories exhibit higher storage density than hard drives with access times close to those of SRAM memories. It has been declared that memristor devices can be scaled down beyond 10 nm^2 and memristor-based

* Corresponding author.
E-mail addresses: hmoustafa@aucegypt.edu, hmostafa@uwaterloo.ca (H. Mostafa).

http://dx.doi.org/10.1016/j.mejo.2016.02.006
0026-2692/

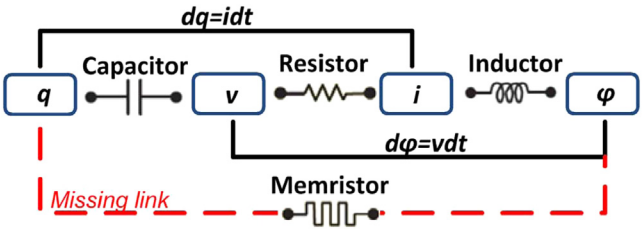

Fig. 1. Four fundamental circuit elements: R, C, L, and M, which is the missing fourth element [1].

memories can achieve high data storage density up to 100 Gbits/cm^2, which is higher than current flash memory technologies [15,16].

Process variation is originated from two main sources: (1) the sub-wavelength lithography process in which the fabricated dimensions are much smaller than the lithography optical source wavelength [17] and (2) the random uncertainties of the dopants atoms which increase as the technology scales [17]. Process variation results in sever fluctuations of the memristor parameters such as width, length, thickness, and device resistivity [18]. This is because the memristor is fabricated at the nano-scale size [19] and is significantly affected by the process variation. For example, the random uncertainties in lithography and patterning processes lead to the random deviations of line edge from its ideal pattern, which is denoted by Line Edge Roughness (LER) [20].

Process variation affects on the memristor-based memories and results in write failure and/or read failure. Write failure occurs when a logic '0' is written into the memory during a write '1' operation and vice versa. Similarly, when the memory provides a '0' in a read '1' operation, a read failure takes place. Throughout this paper, the yield is defined as the probability to write correctly to the memory and to read correctly from the memory. As process variation increases (i.e., as the device gets smaller), the yield is degraded significantly. For example, if the yield is 99.9% this is interpreted as 1 GB memory cells exhibit read and/or write failures in a 1 TB memory.

The rest of the paper is organized as follows. In Section 2, some background is given. The models used for the memristor and the statistical yield simulation setup are discussed in Section 3. Section 4 presents the simulations results and discussions. Some design insights and recommendations for the memristor-based memory designers are given in Section 5. Finally, some conclusions are drawn in Section 6.

2. Background

In the beginning of this background section, it is essential to show the reader the non-volatile emerging memory technologies such as the Phase Change RAM (PCRAM), the Spin-Torque-Transfer Magnetic RAM (STT-MRAM), and the Ferroelectric RAM (FERAM) as listed in Table 1 [21–23]. According to this table, memristor-based memory has better write time and higher density [21,22]. It is clear from this table that the memristor-based memory technology exhibits the highest packing density compared to other emerging non-volatile memory technologies by a factor of 13 × at least. In the meantime, memristor-based memory technology provides comparable read delay, energy per bit, and endurance compared to Phase Change RAM (PCRAM), Spin-Torque-Transfer Magnetic RAM (STT-MRAM), and Ferroelectric RAM (FERAM).

Table 1
Comparison between emerging non-volatile memories [21–23].

Comparison aspect	PCRAM	RRAM (Memristor)	MRAM (STT-RAM)	FERAM
Development	Advanced	Early	Advanced	Advanced
Read time (ns)	12	0.1–10	35	45
Write time (ns)	100	0.1–10	35	65
Energy per bit access (pJ)	100	2	0.02	3.4
Density (Gb/cm^2)	12	154–309	1.2	0.14
Endurance	10^8	10^{10}	$>10^{15}$	10^{15}

2.1. Thin-film memristor

Fig. 2(a) and (b) shows the physical structure of a thin-film memristor device and its equivalent circuit model. The device is composed of a TiO_2 thin film of length D, sandwiched between two metal contacts. There are two layers in the TiO_2 film. One layer is highly resistive pure TiO_2 (un-doped layer), and the other layer is filled with oxygen vacancies, which makes it highly conductive (doped layer). The state variable w represents the width of the doped region. The doped region has low resistance while the un-doped region has much higher resistance.

When an external bias voltage, v, is applied across the device, the electric field repels the positively charged oxygen vacancies from the doped layer into the pure TiO_2 layer and the state length w is changed [3]. Hence, the device total resistivity changes. If the doped region extends to the full length D (i.e., $w/D = 1.0$), the total resistivity of the device is dominated by the low resistivity region and the memristance value is denoted by R_{on}. On the other hand, when the un-doped region extends to the full length D (i.e., $w/D = 0$), the total resistivity of the device is dominated by the high resistivity region and the memristance value is denoted by R_{off}. The mathematical model for Memristive device resistance, M, is given by [5,23]:

$$M(w) = R_{on} \times \frac{w}{D} + R_{off} \times \left(1 - \frac{w}{D}\right)$$
$$\text{where} \quad 0 \le \frac{w}{D} \le 1.0 \tag{1}$$

Fig. 2(c) displays the memristor symbol. The orientation of the symbol follows the equivalent circuit in Fig. 2(b), where R_{on} is on the left hand side and R_{off} is on the right hand side. The polarity is significant in memristor devices which means that if the memristance increases when a positive bias voltage is applied, applying a negative voltage results in reducing the memristance [5,23].

Applying an external bias voltage v results in changing the memristance value as follows [5] assuming the initial condition is R_{on}:

$$M(\phi) = R_{off}\sqrt{\left(\frac{R_{on}}{R_{off}}\right)^2 - \frac{\phi}{\phi_D}}$$
$$\text{where} \quad \phi_D = \frac{(\beta D)^2}{2\mu_v(\beta - 1)} \quad \text{and} \quad \beta = R_{off}/R_{on} \tag{2}$$

where ϕ is the applied external flux and is given by $\phi = \int v \times dt$, μ_v is the average ion mobility, and D is the thin-film memristor thickness. It should be noted that applying a zero average external voltage has no net effect on the memristance value as $\phi = 0$ in this case.

Moreover, in [5], the required flux to switch the memristance value from an arbitrary initial state $M(w_0)$ to a desired state $M(w)$ is given by (i.e., flux controlled memristors):

$$\phi = \frac{\phi_D}{R_{off}^2} \times [M^2(w) - M^2(w_0)] \tag{3}$$