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An optimal linear system approximation of nonlinear fractional-order memristor–capacitor charging circuit

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ABSTRACT

The analysis of nonlinear fractional-order circuits is a challenging problem. This is due to the lack of nonlinear circuit theorems and designs particularly in the presence of memristive elements. The response of a series connection of a simple resistor with fractional order capacitor and its analytical formulation in both charging and discharging phases is considered. The numerical simulation of fractional order HP memristor in series with a fractional order capacitor is also discussed. It is a demonstration of a simple nonlinear fractional-order memristive circuit in both charging and discharging cases. Furthermore, this paper introduces an approach to approximate nonlinear fractional-order memrisitve circuits by linear circuits using a minimax optimization technique. Hence, the new circuit can be analyzed using the conventional linear circuit theorems. The charging and discharging of a series fractional-order memristor with a fractional-order capacitor are discussed numerically. The effect of fractional-order parameters and memristor polarity are also investigated. Using a suitable optimization technique, an accurate approximation by a circuit that include a resistor and a fractional-capacitor is obtained for both charging and discharging cases. A great matching was observed between the frequency responses of the fractional-order nonlinear low pass filter based on fractional-order memristor and fractional-order capacitor and that of the optimized linear fractional order case. Similar matching is observed for the nonlinear and optimized cases when a periodic triangular waveform is applied using Fourier series expansion.

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1. Introduction

Recently, memristive-based circuits have been a spirited exploration area in different applications based on the new fundamentals of these memory-dependent nonlinear elements. Previously, the three conventional two-terminal elements, the resistor (R), the capacitor (C), and the inductor (L) were the leading elements to constitute the linear circuit theory, which affects all current applications.

The history of memristive elements goes back to 1971 when Leon Chua postulated the missing relation between the charge and flux, and hence the memristor (memory-resistor) was introduced [1]. But substantial attention towards this invention was achieved once the first memristor was physically implemented by the Hewlett Packard laboratories [2] in 2008. The main fundamentals of this HP-nonlinear two-terminal passive element are its size, that is 10 nm, and the fact that it has pinched frequency-dependent hysteresis $i-v$ characteristics.

The HP-memristor [2] was built on drifting the dopant between doped and undoped portions of the material as shown in Fig. 1(a). The instantaneous resistance of the memristor is given by [2]:

$$R_m(x) = xR_{on} + (1-x)R_{off}, \quad x = \frac{w}{L}, \tag{1}$$

where R_{on} is the resistance of the completely doped memristor, R_{off} is for the completely undoped and w is the length of the doped region, which is bounded between 0 and the device length L. The speed dopant movement is defined as:

$$\frac{dx}{dt} = ki(t)f(x), \quad k = \frac{\mu_v R_{on}}{L^2}, \tag{2}$$

where $f(x)=1$ in the linear dopant drift model [3]. The instantaneous resistance of the memristor subjected to input voltage $v(t)$ is given by [4]:

$$R_m^2 = R_0^2 - 2k(R_{off} - R_{on})\int_0^t v(\tau)d\tau, \quad R_m \in (R_{on}, R_{off}), \tag{3}$$

where R_0 is the initial resistance at $t=0$. Fig. 1(b) shows the current–voltage pinched hysteresis under sinusoidal input voltage of 1 Hz frequency and 1 V peak voltage, and memristor parameters R_{off}, R_{on}, R_0 are equal to 38 kΩ, 100 Ω, 4 kΩ respectively. Due to the fact that memristor is still unavailable commercially, many memristor-

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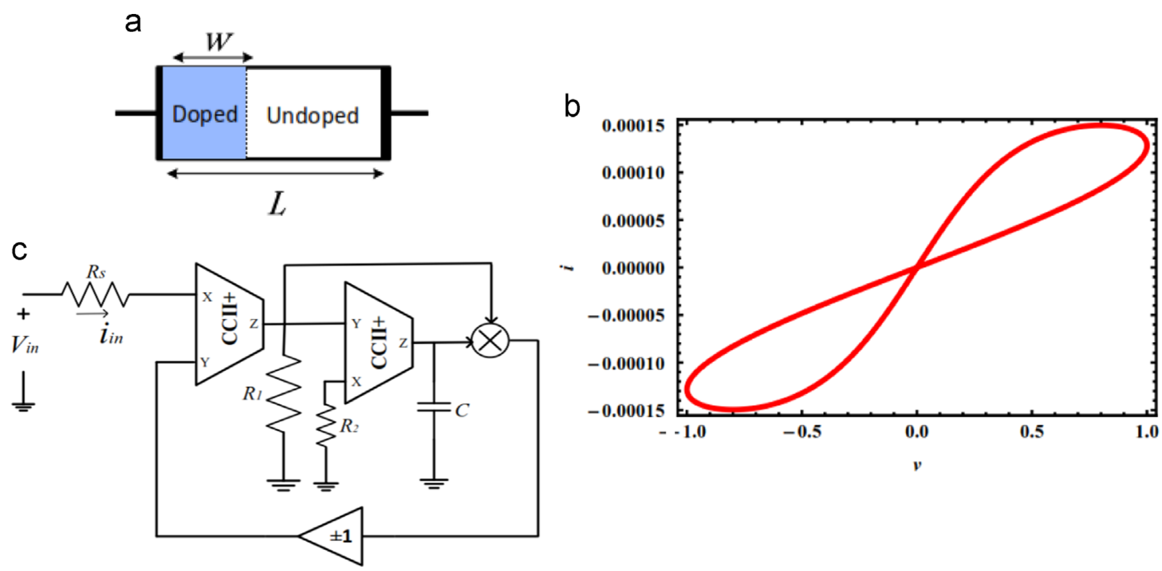

Fig. 1. (a) The abstract structure of the HP-memristor, (b) memristor current versus input sinusoidal wave voltage, and (c) current-controlled decremental/incremental memristor emulator.

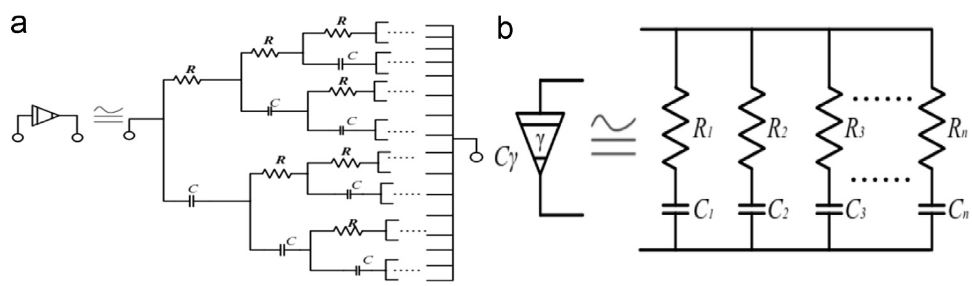

Fig. 2. (a) Finite element approximation of a fractal capacitor of order 0.5, and (b) approximation of a fractal capacitor of any order $\alpha < 1$.

emulator circuits have been recently proposed in [5,6]. The emulator circuit is based on the current-controlled memristor which consists of two current conveyor (CCII+) devices, a voltage multiplier and a noninverting or inverting buffer [6,7] as shown in Fig. 1(c). Although the memristor has many advantages due to its size, memory, and dynamics behavior, it is a nonlinear element where the conventional linear circuit theorems cannot be applied.

During the last few years, hundreds of research projects, patents and papers were proposed to study and investigate memristor-based applications in different fields: analog circuits [8,9], oscillators [10,11] and digital circuits [12]. Moreover during the last few decades, fractional-order systems find extensive use in different engineering applications [13] such as circuit theory, biomedical field, control, and electromagnetics. Many theorems and generalized fundamentals have been introduced using fractional-order circuits such as fractional-order oscillators, filters and 3D Smith chart [14–16]. The main fractional-order definition is known as Riemann–Liouville fractional integral operator (J^{α}) of order $\alpha \geq 0$ and is given by [17]:

$$J^{\alpha}f(t)=\begin{cases}\frac{1}{\Gamma(\alpha)}\int_0^t (t-\tau)^{\alpha-1}f(\tau)d\tau, & \alpha>0\\ f(t), & \alpha=0\end{cases}. \tag{4}$$

However, the most well-known fractional-order derivative D^{α} of $f(t)$ is known as Caputo definition and is given by:

$$D^{\alpha}f(t)=\begin{cases}\frac{1}{\Gamma(m-\alpha)}\int_0^t (t-\tau)^{m-\alpha-1}f^{(m)}(\tau)d\tau, & m-1<\alpha<m\\ f^{(m)}(t), & \alpha=m\end{cases}, \tag{5}$$

where its left-fractional-integral is given by:

$$J^{\alpha}D^{\alpha}f(t)=f(t)-\sum_{j=0}^{m-1}f^{(j)}(0)\frac{t^j}{j!}. \tag{6}$$

The Laplace transform of fractional derivatives of order α under zero initial conditions is given by:

$$\mathcal{L}\{D^{\alpha}f(t)\}=s^{\alpha}F(s). \tag{7}$$

Several authors suggested the feasibility of realizing a fractional-order capacitor [18–22]. In [19], authors proposed a finite element approximations technique to emulate a fractional-order capacitor with order 0.5 via semi-infinite self-similar RC trees as shown Fig. 2(a). This technique was later developed in [20–22] for any order. The finite element approximations of fractional order capacitor are shown in Fig. 2(b). Also, the fractional-order memristor model was recently introduced in [23,24] which generalizes the state equation of the HP-memristor into the fractional-order sense. Although this model increases the design flexibility by the added fractional-order parameter which is desired for many recent applications, the analysis of memristor-based circuits based on this model is complicated because its mathematical representation is that of a system of nonlinear fractional-order differential equations.

In this paper, the discussion of the basic charging/discharging series fractional-order memristor with fractional-order capacitor [25,26] is presented by solving numerically its nonlinear fractional order differential equation using the predictor–corrector method [27]. A multi-objective minimax optimization problem is formulated to approximate this nonlinear circuit by a linear circuit that consists of a resistor with a fractional-order capacitor. This optimization problem tries to find the best parameters in the linear circuit that match the

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