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Noise minimization limits in multichannel integrated circuits dedicated to neurobiology experiments

P. Kmon

AGH University of Science and Technology, Faculty of Electrical Engineering, Automatics, Computer Science and Biomedical Engineering, Department of Measurement and Electronics, al. A. Mickiewicza 30, 30-059 Krakow, Poland

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ABSTRACT

The paper presents an analysis of problems associated with the area and power reduction of readout circuits used in multichannel neurobiology experiments, in relation to noise minimization. The noise limits of a single channel considered as a function of the silicon occupation and power consumption are analyzed for an amplifier working with capacitive feedback. The paper also presents an efficient method of noise minimization in multichannel recording systems used in neurobiology experiments, when the power budget and silicon area per single recording channel are strictly limited. The proposed idea was verified in an eight-channel prototype integrated circuit fabricated in CMOS 180 nm process. The prototype IC measurements show that with the use of the proposed method, one can decrease the recording channels' noise two times with the existing dedicated power and area budget.

1. Introduction

Currently, there is a great demand to develop implantable integrated circuits that would combine recording electrodes and multichannel recording electronics, and would incorporate hundreds of recording sites. It is anticipated that such systems will be used in both implants for people with disabilities and to explore unknown nervous system organization [1–3]. The more recording sites of such a system, the better the understanding of observed phenomena. This leads to the requirement of multichannel architectures of readout systems. Beside its main parameters, such as low power consumption (below 10 μW/channel), small area occupation and large functionality (programmable recording bandwidth and voltage gain, on-chip data compression, telemetry link for power and data transmission, electrical stimulation), Input Referred Noise (IRN) is one of the most important parameters. And with the tight area and power limitations expected from future integrated neurobiology systems, noise minimization becomes ever more challenging task.

Multichannel systems often have a pixel-like segmented architectures (see Fig. 1) and consist of tens of active sites. These are built of integrated circuits (IC) combined with recording electrodes that, during the experiment, are placed close to the neural networks. Signals that are being recorded depend on a particular experiment. Many neurobiology explorations are carried out to record Local Field Potentials (LFP) and Action Potentials (AP) that are different in frequency band and amplitude. The frequency band of the LFP signals is from below 1 Hz to 500 Hz while AP signals are from about 300 Hz to 7 kHz. LFP amplitudes span from below 10 μV to 5 mV and AP from below 10 μV to 500 μV.

There are many distinctive IC examples of pixel shaped organization, both dedicated for in vivo and in vitro experiments [4–9]. To verify the design efficiency of these types of amplifiers the NEF (Noise Efficiency Factor) is used, which combines an amplifier's noise, its current consumption and frequency bandwidth [10]:

$$\mathrm{NEF} = \mathrm{IRN}\sqrt{\frac{2I_{TOT}}{\pi \cdot \varphi_T \cdot 4kT \cdot BW}} \tag{1}$$

where I_{TOT} is the total current consumed by the amplifier, φ_T is the thermal voltage, k is the Boltzmann constant, T is the temperature, and BW is the amplifier's bandwidth.

The NEF parameter provides the ability to compare different recording channel designs in terms of IRN, BW and I_{TOT} but it does not allow comparison of design efficiency in terms of area occupation per single channel. However, it is well known that both the area and power have a major influence on the IRN of an amplifier. Nowadays, ICs of pixel architectures dedicated to implantable systems have no more than 100 recording channels. Increasing the number of channels results in a decrease not only of power consumption per channel but also of silicon area per channel and both these factors negatively influence the overall IRN. However, neurobiologists are looking for next generation of recording systems

E-mail address: kmon@agh.edu.pl

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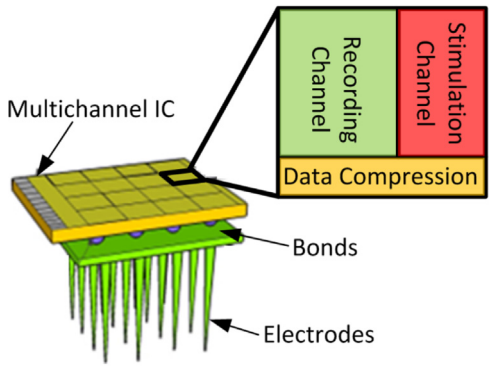

Fig. 1. Conceptual scheme of the multichannel system dedicated to neurobiological experiments.

capable of recording activity from several hundred to a few thousand neurons simultaneously.

It is for this reason the article provides analysis that shows recording channels' noise minimization limits in respect to strict power and area constraints. Additionally, an efficient area and power utilization method is proposed as one option for mitigating the IRN deterioration with the effect on the area and power minimization. The method proposed can be used in ICs that consist of hundreds of recording channels, especially within implantable ICs where one has to utilize allowable power and area budget efficiently.

The paper is organized in the following way: Section 2 deals with the IRN analysis of a recording channel. Section 3 describes the proposed method employed in the IC. Section 4 consists of measurement results, while Section 5 concludes the paper.

2. IRN analysis of the recording channel

In the development of multichannel implantable systems to be combined with recording electrodes, the amplifier area occupation and power consumption are among the most important parameters. One can see an instructive review of possible solutions [11]. It is evident that these parameters have a major influence on the IRN of the recording channel. Therefore, bearing in mind these parameters, an amplifier with capacitive gain elements is analyzed (see Fig. 2). The main reason for considering this particular amplifier was the fact that its architecture is attractive in terms of simplicity of implementation, power dissipation, noise and input dynamic range and it has an inherent AC coupling at the input [9]. As a result, it is extensively used to amplify and filter weak neurobiology signals [4–9]. Here the core of the amplifier is based on a differential OTA (Operational Transconductance Amplifier).

Amplifiers' main parameters, such as voltage gain K_V gain and lower corner frequency f_{Low}, are defined by passive components (see Fig. 2). The electrode's parameters depend mainly on the experiment and may be assumed to have an impedance on the range of hundreds of kΩ to a few MΩ at a frequency of 1 kHz. In this paper only the noise of the amplifier is taken into account in order to provide information on its relation to the silicon area and power consumption. The simplified scheme of the amplifier also contains the main noise sources that refer to the resistors $\overline{i_R^2}$ and amplifier's core $\overline{v_{CORE}^2}$. The IRN of the amplifier can be related to the amplifier's core noise contribution IRN_{CORE} and to the noise contributed by the resistors IRN_R:

$$\mathrm{IRN} = \sqrt{\mathrm{IRN}_{CORE}^2 + \mathrm{IRN}_R^2} \tag{2}$$

Here, the IRN_{CORE} and IRN_R components are analyzed separately in terms of area and power restrictions.

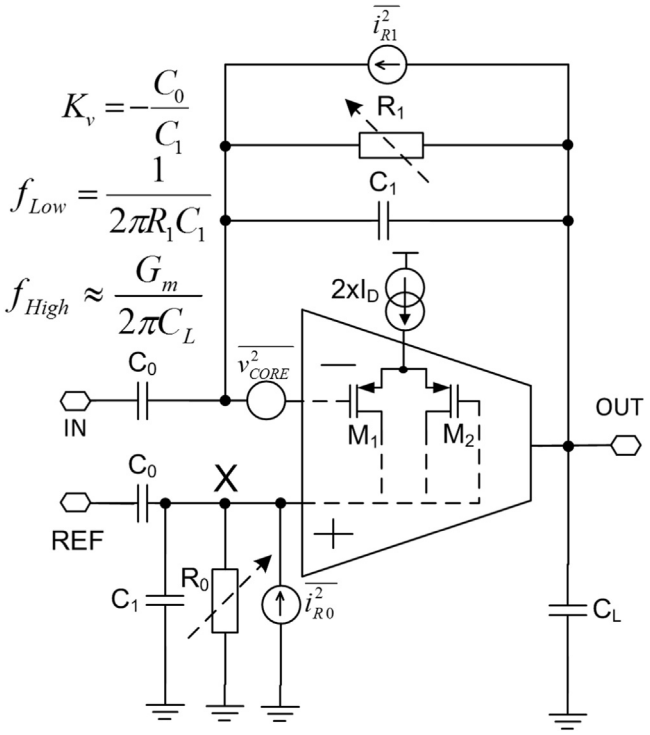

Fig. 2. Simplified scheme of the amplifier including main noise sources.

To illustrate the existing limits of the amplifier architecture in figures, the following assumptions were taken into account:

- The amplifier was set to record both LFP and AP signals, i.e. its bandwidth was set to 0.1 Hz to 7 kHz, while its voltage gain was set to 100 V/V,
- The area occupied by a single recording channel was equal to the area of the employed capacitors as most current technologies allow for placing capacitors above active circuitry (i.e. the core of the amplifier is placed below capacitors). The capacitance/area ratio was assumed to $c = 1$ fF/μm^2 (it is a reasonable assumption for most available technologies). Therefore, the total area occupied by the recording channel was approximately $2(C_0+C_1)/c$, which may be assumed as $2C_0/c$ (because the $C_0 \gg C_1$ for assumed voltage gain).

2.1. Resistor's noise contribution

The noise contribution from resistive elements was taken into account in terms of area occupied by the amplifier. In the proposed preamplifier architecture one has to take into account resistors R_0 and R_1. The resistor R_0 forms a filter with capacitors C_0 and C_1. It may be assumed that its corner frequency is determined by the R_0C_0 time constant because $C_0 \gg C_1$. The resistor R_1 is connected in parallel to capacitor C_1. Values of both resistors are equal ($R_0 = R_1$) but they are connected in parallel to different capacitors values and located in different preamplifier's sections. However, it is shown below that both resistors noise contributions may be assumed equal.

To calculate R_0 noise contribution one has to take into account the amplifiers' bandwidth. Then, its noise may be referred to the amplifier's output as:

$$\overline{v_{nR0}^2} = \int_0^\infty \frac{4kTR_0}{\left|1 + j2\pi f R_0 C_0\right|^2} \times \left|H(f)\right|^2 df \tag{3}$$