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Thermal stability of sectorial split-drain magnetic field-effect transistors

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ABSTRACT

The effect of charge trapping on the performance of sectorial Split-Drain Magnetic Field Effect Transistor (SD-MAGFET) under the influence of magnetic field is examined based on conventional capacitance measurement techniques upon different magnetic field strength and thermal conditions. The experimental results confirmed the charge trapping effect in sectorial SD-MAGFET is magnetic field and temperature dependent, where the charge trapping sites are localized at the channel boundary, which verifies the conjecture of trap-assisted magnetic sensitivity hysteresis and deterioration of the device found in recent literatures. The results of the study are useful to sectorial SD-MAGFET in high performance magnetic sensing applications.

1. Introduction

Split-Drain Magnetic Field Effect Transistor (SD-MAGFET) manufactured with conventional CMOS compatible process has been a promising candidate to the magnetic sensor that can integrate with other circuits on a single chip [1,2]. The SD-MAGFET can be fabricated with different shapes (with respect to the channel), such as rectangular, sectorial, and circular, etc., where the sectorial SD-MAGFET is shown to be able to achieve the best magnetic sensitivity with a given silicon size [3–5]. However, their applications have been limited by unknown sensitivity limitation and deterioration. Recent publications have shown that the sensitivity limitation and deterioration are geometric dependent [4,5], and they are caused by trapped charges [6]. The magnetic stressing study in Ref. [7] shows that the performance of the sectorial SD-MAGFET would be affected by charges trapped on the channel sidewall. However, there has been insufficient information to pinpoint the location of charge trapping that affects the operation of the sectorial SD-MAGFET.

It is the objective of this study to provide additional evidence on the location of charge trapping that affects the performance of the sectorial SD-MAGFET under the influence of an external magnetic field. We shall study the inference of charge trapping on sectorial SD-MAGFET through measuring the gate-to-drain capacitance (C_{gd}) of sectorial SD-MAGFET with a low voltage to bias the gate-to-drain interface under the influence of an external magnetic field. The C_{gd} is studied because when the biasing voltage between gate-to-drain is low, the only possible location for charge trapping is the channel sidewall which is also known as the channel boundary. Therefore, our study will help to pinpoint where the charge trapping occurs in the sectorial SD-MAGFET under the influence of an external magnetic field. We shall further study the geometric dependence of the amount of charge trapping in sectorial SD-MAGFET under the influence of external magnetic field. Our study shall conclude with a discussion on such geometric dependence and it's implication on the application of sectorial SD-MAGFET as magnetic sensor in real world.

2. Channel boundary charge trapping

Showing in Fig. 1 is the micrograph and layout of a sectorial SD-MAGFET that we shall study in this paper, where similar devices have been studied in [6,7]. The device under study is an N-channel sectorial SD-MAGFET which consists of a source terminal (Source) and two drain terminals (Drains 1 and 2). The darker gray color region in the figure identifies the channel region, while the lighter gray color regions identify the source and drain regions. The arc of the overlap sector of the gate and drain terminals is the channel width W of the sectorial SD-MAGFET. The channel length, the radius of the source terminal, the spacing between the two drain terminals, the drain channel overlap, and the angle sustained by the sectorial SD-MAGFET are denoted as L, R, d, u and α, respectively. When a magnetic field B is applied perpendicular to the channel (as indicated by the cross in the figure), a Lorentz force will be induced that deflects the electrons in the channel from reaching Drain 2 to Drain 1, and thus creates a differential current known as the Hall current [2] given by $\Delta I_H = I_{DS1} - I_{DS2}$, where I_{DS1} and I_{DS2} are the drain currents measured at Drains 1 and 2, respectively.

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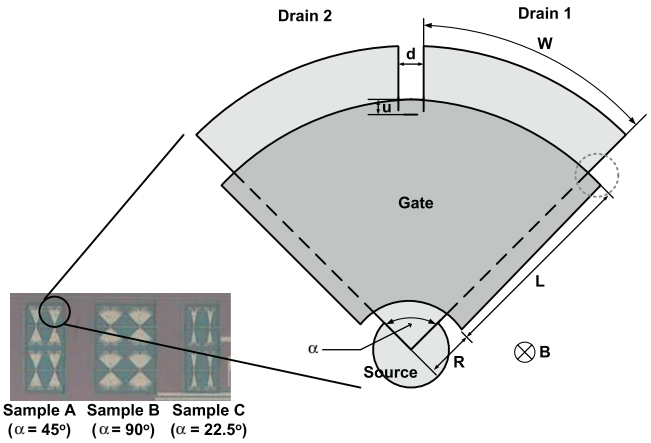

Fig. 1. Layout and micrograph of the N-channel sectorial SD-MAGFETs under investigation, where the location of the charge trapping without active channel is enclosed by the circle in dotted line.

When the carriers in the sectorial SD-MAGFET channel are deflected sideway by the magnetic field, they not only generate the Hall current ΔI_H, there are also chances that they may get trapped in the interface states and affect the performance of the sectorial SD-MAGFET.

One of the common methods to extract the channel boundary interface charge trapping is to study the C_{gd} variation under the influence of an external magnetic field. Showing in Fig. 2(a) and (b) are the equivalent models of the gate-to-drain capacitance C_{gd} with the gate-to-drain interface in sectorial SD-MAGFET biased to accumulation and depletion, respectively. We shall use $C_{gd,acc}$ and $C_{gd,dep}$ to denote the C_{gd} in accumulation and depletion, respectively. In particular we are interested in the variation of capacitance ΔC given by

$$\begin{aligned}\Delta C &= C_{gd,dep} - C_{gd,acc} \\ &= C_{bot} + \frac{C_{sw}C_{trap}}{C_{sw}+C_{trap}},\end{aligned} \tag{1}$$

where

$$C_{gd,acc} = C_{ov}, \tag{2}$$

$$C_{gd,dep} = C_{ov} + C_{bot} + \frac{C_{sw}C_{trap}}{C_{sw}+C_{trap}}, \tag{3}$$

are composed with the overlap capacitance C_{ov}, drain bottom to substrate capacitance C_{bot}, channel sidewall capacitance C_{sw}, and capacitance associated with trapped charges C_{trap}. Without loss of

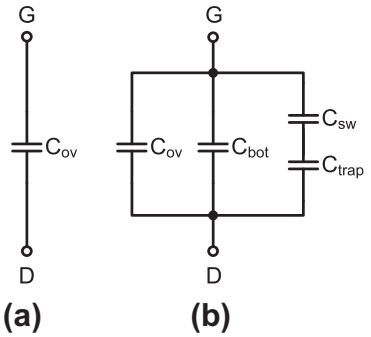

Fig. 2. Equivalent capacitance model of the gate-to-drain interface of the sectorial SD-MAFET in (a) accumulation and (b) depletion modes, where C_{ov}, C_{bot}, C_{sw}, and C_{trap} are the overlap capacitance, drain bottom to substrate capacitance, channel sidewall capacitance, and capacitance associated with trapped charges, respectively.

generality, C_{bot} and C_{sw} can be assumed to be constant under small biasing voltage across gate and drain, room temperature, and external magnetic field. As a result, the larger C_{trap}, the larger ΔC. Therefore, the study of the variation of the differential capacitance between the accumulation and depletion C_{gd} will be a good measurement.

It should be noted even though there is no drain current (when no active channel formed in SD-MAGFET), carriers would keep diffusing in the drain regions. Since defects are intrinsic, the carriers would have the chance to get trapped or de-trapped at the defect sites through diffusion. The magnetic field induced Lorentz force deflects the carrier sideway to the overlap interface of the drain terminals and the gate regions (i.e. the channel boundary located at channel end, see the circle region in Fig. 1). Therefore, the charge trapping behavior under the influence of magnetic field at this region can also be applied to the overlap interface region across the whole active channel. We further conjectured that such behavior will be exaggerated with increasing channel length, which would affect the magnetic sensitivity of the SD-MAGFET due to charge trapping. A similar study on the dependence of channel length on magnetic sensitivity in SD-MAGFET has also been reported, however, the underneath physical phenomenon has not been fully exploited [4,8]. The following section will describe the experiment that we have carried out to measure ΔC for the confirmation of the above discussions.

3. Experiment

Three N-channel sectorial SD-MAGFETs fabricated on 2.25 μm Metal Gate process as shown in Fig. 1 with different sector angles and geometric parameters summarized in Table 1 were investigated. The same set of samples have been investigated in [6,7]. To mitigate the adverse effect of layout mismatch and measurement noise, eight sectorial SD-MAGFETs with the same geometric parameters were cross-couple connected to form an equivalent sectorial SD-MAGFET, such that the measured C_{gd} will be larger than the minimum measurement limit of our equipment.

The C_{gd} of the sectorial SD-MAGFET can be measured in a similar manner as that of the conventional MOSFET. Fig. 3 shows the schematic of the experiment, where the capacitance variation was measured by HP Precision LCR Meter HP4284A with the gate and Drain 1 of the sectorial SD-MAGFET connecting to the "HIGH" and "LOW" terminals of the LCR meter, respectively. The source and P-substrate of the sectorial SD-MAGFET were internally connected and coupled to the ground for better noise immunity. The measurement is performed with Drain 2 of the sectorial SD-MAGFET at float. The "HIGH" terminal voltage varies from -6 V to +6 V with respect to the "LOW" terminal, such that the gate-to-drain interface can be biased into different modes according to the difference voltage between the gate-to-drain interface (i.e. V_{gd}). When $V_{gd} \leqslant 0$ V, the gate-to-drain interface is biased at accumulation and the measured $C_{gd} = C_{gd,acc}$. When $V_{gd} \geqslant V_{th,n}$ =0.6 V, the gate-to-drain interface is biased at depletion and the measured $C_{gd} = C_{gd,dep}$, where $V_{th,n}$ is the typical threshold voltage of the sectorial SD-MAGFET under investigation. To investigate the variation of C_{gd} under the effect of magnetic field strength at different tem-

Table 1
Geometric parameters of the sectorial SD-MAGFETs.

Sample No.	A	B	C
Channel length L (μm)	49	49	49
Radius of source R (μm)	10	10	10
Sector angle α (degree)	45	90	22.5
Drain separation d (μm)	3	3	3
Drain channel overlap u (μm)	1	1	1