Microelectronics Reliability 54 (2014) 1412–1420

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Soft error estimation and mitigation of digital circuits by characterizing input patterns of logic gates

Siavash Rezaei [a,*], Seyed Ghassem Miremadi [a], Hossein Asadi [a], Mahdi Fazeli [b]

[a] Department of Computer Engineering, Sharif University of Technology, Tehran, Iran
[b] Department of Computer Engineering, Iran University of Science and Technology, Tehran, Iran

ARTICLE INFO

Article history:
Received 29 May 2013
Received in revised form 4 February 2014
Accepted 3 March 2014
Available online 3 April 2014

Keywords:
Soft errors
Single event transient
Multiple event transient
Radiation hardening
Gate sizing

ABSTRACT

Soft errors caused by particles strike in combinational parts of digital circuits are a major concern in the design of reliable circuits. Several techniques have been presented to protect combinational logic and reduce the overall circuit *Soft Error Rate* (SER). Such techniques, however, typically come at the cost of significant area and performance overheads. This paper presents a low area and zero-delay overhead method to protect digital circuits' combinational parts against particles strike. This method is made up of a combination of two sub-methods: (1) a SER estimation method based on signal probability, called *Estimation by Characterizing Input Patterns* (ECIP) and (2) a protection method based on gate sizing, called *Weighted and Timing Aware Gate Sizing* (WTAGS). Unlike the previous techniques that either overlook internal nodes signal probability or exploit fault injection, ECIP computes the sensitivity of each gate by analytical calculations of both the probability of transient pulse generation and the probability of transient pulse propagation; these calculations are based on signal probability of the whole circuit nodes which make ECIP much more accurate as well as practical for large circuits. Using the results of ECIP, WTAGS characterizes the most sensitive gates to efficiently allocate the redundancy budget. The simulation results show the SER reduction of about 40% by applying the proposed method to ISCAS'89 benchmark circuits while imposing no delay overhead and 5% area overhead.

1. Introduction

The collision of alpha and neutron particles to a semiconductor device may generate a track of electron–hole pairs. The possible existence of electric field in off-state transistors causes electrons and holes move in the opposite directions [1–3]. This generates an unwelcome transient current pulse which may charge or discharge the load capacitance of a single or multiple gates causing either *Single Event Transient* (SET) or *Multiple Event Transients* (METs) [4]. If a particle directly strikes the sensitive nodes of memory elements, it may change the stored value depending on the amount of deposited charge, resulting in either *Single Event Upset* (SEU) or *Single Event Multiple Upset* (SEMU) [5]. Any unwelcome bit-flip in memory elements due to these phenomena is referred to as soft error.

Although SEUs were previously the major concern in digital circuits, with emerging nanoscale dimensions, SETs and METs have become the dominant threat to the reliability of digital circuits due to two main reasons. First, the occurrence rate of SEUs in sequential parts (memories and latches) has been approximately constant over several technology generations; while technology scaling extremely increases the occurrence probability of SETs/METs in combinational parts [6]. Second, there are two main approaches that can effectively protect sequential parts against SEUs: (a) *Error Detection And Correction* (EDAC) codes which are a viable solution to protect sequential parts such as cache or register file against SEUs [4,7], and (b) hardening approach such as hardened latch [8], hardened flip-flop [9], and hardened SRAM [10]; the former approach, i.e., the EDAC codes, cannot be applied to detect SETs/METs and the latter approach, i.e., the use of radiation hardened elements, would result in a significant area, power, and delay overheads since the number of gates in a digital circuit is much greater than sequential cells.

Hardening of combinational parts can be done by two main approaches: (1) enhancement of the inherent masking capabilities of circuits, i.e., logical masking, electrical masking, and latching-window masking. In this approach, the masking factors inherently prevent SETs/METs either propagating in combinational logic or being latched in sequential elements [11]; the main shortcoming of this approach is imposing significant performance degradation.

* Corresponding author. Tel.: +98 9183668185.
E-mail addresses: srezaei@ce.sharif.edu (S. Rezaei), miremadi@sharif.edu (S.G. Miremadi), asadi@sharif.edu (H. Asadi), m_fazeli@iust.ac.ir (M. Fazeli).

http://dx.doi.org/10.1016/j.microrel.2014.03.003
0026-2714/

(2) selectively hardening of a subset of elements to prevent transient pulses to being generated [12,13,6]. In this approach, to achieve the best hardened circuit for a certain amount of overheads, an accurate comparative estimation of gates sensitivity as well as an appropriate allocation of redundancy budget to the selected elements are required. To the best of our knowledge, none of the previous selective hardening methods has proposed a practical approach to compute the probability of transient pulse generation in large circuits. The only well-known approach to compute this probability is based on fault injection which is not tractable for large circuits.

This paper presents an analytical *Soft Error Rate* (SER) estimation method followed by a low area and zero-delay overhead method to protect combinational logic against particles strike. The main contribution of this paper can be discussed in two major parts as in the following.

1. SER estimation: this paper presents a detailed study supplemented with extensive simulation results to demonstrate the inaccuracy due to ignoring the effect of input patterns in transient pulses generation. Based on this fact, we propose an analytical method to determine circuits' SER by characterizing the circuits' nodes signal probability. We call this method *Estimation by Characterizing Input Patterns* (ECIP).
2. SER mitigation: we have demonstrated that the signal probability of internal nodes has a significant effect on selective hardening methods. Hence, we leverage this fact to determine the most sensitive circuit's gates and protect them by using our proposed gate sizing algorithm (called *Weighted and Timing Aware Gate Sizing* (WTAGS) which is a combination of the best characterizations of previous gate sizing methods). Finally, we investigate the impact of the input reordering technique beside WTAGS with different orders to achieve higher level of protection.

The main aim of the proposed method is to enhance the reliability of target circuits considering limited area and/or delay overheads. To this end, we try to efficiently assign the available overhead to achieve the highest possible reliability. The proposed method is applied to ISCAS'89 benchmark circuits using the Nangate 45 nm technology library [14]. The efficiency of the proposed method is evaluated by using a combination of HSPICE simulations and statistical analysis. The results demonstrate on average 40% SER reduction with 5% area overhead and no performance penalty.

The rest of this paper is organized as follows. In Section 2, we present an overview of previous research on SET modeling and the previous work on SER reduction. Section 3 presents the proposed method, i.e., ECIP and WTAGS. The simulation setup and the simulation results are given in Sections 4 and 5, respectively. Section 6 discusses the limitations of the proposed method and possible extension of this work. Finally, Section 7 concludes the paper.

2. Related work

Before discussing the previous works on SER mitigation techniques, it is necessary to explain how the effect of a particle strike on a sensitive node of a circuit can be modeled. This effect can be modeled as a single or a double exponential time-dependent current pulse (injecting into the victim transistors drain) [15]. The double exponential model has been widely used to model an alpha particle strike [16] while the single exponential model is more accurate to model a neutron particle strike [17]. We have used the single exponential model shown in (1) in our experiments, however, this does not affect the effectiveness of the proposed methods.

$$I(t) = \frac{2 \times Q}{\tau_\alpha \times \sqrt{\pi}} \times \sqrt{\frac{t}{\tau_\alpha}} \times \left(e^{\frac{-t}{\tau_\alpha}}\right) \quad (1)$$

In this equation, Q is the amount of charge deposited by the strike of a particle and τ_α is the charge collection time constant of the p–n junction (a CMOS technology process-related factor).

Generally, SET mitigation can be done using the following approaches:

1. Reducing the probability that transient pulses result in soft errors, i.e., trying to prevent transient pulses to be latched by circuit bistables. This can be achieved mainly by increasing the capability of a circuit to mask transient pulses by logical, electrical, or latching-window masking factors.
2. Reducing the probability of transient pulse generation. This approach includes gate or transistor resizing and/or reordering techniques.

In the next subsections, we review these two categories in detail.

2.1. SER Mitigation by Enhancing Masking Factors

Inserting a filtering circuit into some paths of a digital circuit is the main idea of the circuit level methods presented in [18–23]. This increases the effect of electrical masking in the modified paths. A major disadvantage of such methods is introducing new susceptible regions to the combinational parts. Furthermore, inserting the filtering circuits in an internal node of a circuit imposes significant performance degradation if the target nodes rely on the circuit critical path.

The method presented in [9] have focused on increasing the probability of latching-window masking by proposing a circuit inserted in the clock input of memory elements. The proposed circuit prevents a SET with a pulse width less than a certain threshold value to be latched by regulating the clock edge timing. However, regulating the clock edge timing at sub-threshold voltages may make the design unreliable. In [24], a method has been presented which increases the effect of latching-window masking by using data multiple clocking. This method is based on a *Triple Modular Redundancy* (TMR) technique that votes between three different memory elements taking three different samples of data in different time slices. However, producing shifted clock pulses for redundant memory elements needs a relatively complex circuit. In addition, the voter circuitry in this method is a single point of failure. Lastly, this method introduces a significant amount of performance degradation and area overhead to the circuit.

2.2. SER Mitigation by Reducing Pulse Generation Probability

The most common point in fault avoidance based methods is gate sizing. When the dimension of a transistor is increased, because of enlargement of parasitic capacitances and augmentation of transistor current drive, the critical charge (Q_{Crit}) of transistor increases; consequently, the device would become more robust against particles strike. The critical charge of a transistor in a logic gate is the minimum amount of charge that if injected into the drain of that transistor, a transient voltage pulse is generated at the output of the gate. However, applying the gate sizing method to all logic gates imposes a significant amount of area and performance overhead. On the other hand, it has been shown that the origin of more than 80% of soft errors is only 50% of the gates [25]. Therefore, the gate sizing method can be used selectively. Thus, one of the most problematic challenges in utilizing the gate sizing method is determining the critical gates to achieve the maximum reduction of SER for limited amount of area and/or performance overhead budget.

There are several works that have tried to reduce the SER of combinational circuits using the gate sizing method