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Design-in-reliability: From library modeling and optimization to gate-level verification

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ABSTRACT

A novel and comprehensive framework for aging analysis is presented in this work, comprehending degradation from BTI, hot-carriers and electro-migration. For the first time, all the primary variables affecting the aging of an interconnect and the transistor – namely, the equivalent duty-cycles, slews and frequencies are incorporated into the calculation. Additionally, from electro-migration stand-point, the framework allows calculation of the exact RMS and 'recovered' average current for every metal segment internal to the circuit, thus making it practically a universal model for aging analysis. Through detailed waveform-processor developed for validation, the aging model is ensured to be within 5% of exact SPICE calculations.

The immediate application of such an extensive and accurate modeling is drawn in terms of influencing changes to the library design/architecture itself, showcased through circuit and layout optimization from EM, hot-carriers and NBTI constraints. Finally, we demonstrate the ultimate benefit from such a library model for doing exact gate-level aging analysis, as well as against asymmetric aging. Results from 28 nm production library models and complex SoC are shared.

1. Introduction

Negative Bias Temperature Instability (NBTI), or gradual degradation of pMOS transistor and Channel Hot Carrier (CHC), are dominant product aging mechanisms. Their analysis and containment, in forms of manufacturing process correction, test guard-bands, designs margins and techniques has been an integral part of chip making, since last decade [1–4]. State-of-the-art STA methodologies for aging, are reasonable in capturing the circuit's response to BTI – which is a very strong function of the operating conditions: the input slew, output load. However, the degradation as a phenomenon is strongly dependent on the operating voltage, temperature and ON-time of 'a' transistor – in turn dependent on the overall history of the circuit operation, the toggle and slew rates at the inputs and the loading condition.

Clearly, on a chip having multi-million transistors, the simplistic STA methods break, leading to significant inaccuracies in aging analysis. A simple extension of the problem is highlighted through Fig. 1 in form of clock-network's asymmetric aging based on the clock input states – analysis of which is not possible through standard methodologies. Such scenarios only aggravate with aggressive usage of power management techniques [1,15,16].

Needless to say, all of these warrant a tight skew as well as pulse-width control from aging stand-point, including accurate comprehension of circuit activity to the internal nodes.

Moreover, looking at the phenomenon of NBTI or CHC in a standard 3-input AND circuit of Fig. 2a, for the encircled pMOS transistor (Fig. 2b), traditional wisdom holds that pMOS degradation happens in the logical '0' regime. However, we note that the 'maximal' NBTI degradation really happens in the non-slew regime of the waveforms (Fig. 2c). Thus it is needed to incorporate slew effects into NBTI induced delay degradations. Very naturally, such a dependence of NBTI effect on the gate-slew also brings in the dependence on the switching frequency through every input of the cell. Thus we present a novel methodology of building libraries by means of delay-arc-wise sensitivities for each transistor, as a function of toggle rates and static probabilities of all inputs.

In real circuits, however, it is not just the transistor which undergoes aging. Electromigration (EM), in wires has only aggravated in past two decades with exponential shrinkage in wire-sizes and much higher increase in the current densities. Much of the EM problem revolves around containing the average and RMS current densities in interconnects – namely signals, power network and cell-internal. While several enhancements happened in EM analysis

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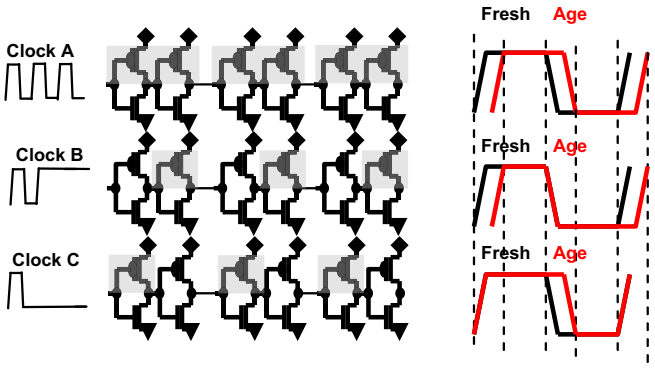

Fig. 1. Schematics and degradation-maps of (A) free running clock, (B) gated-high clock and (C) a gated-low clock, along with fresh/aged waveforms.

flow in past years – including accurate signal and power network current estimation, what remained unsolved and inadequately handled is the cell-internal EM checking portion at SoC level.

Through this work, we extend our novel methodology to accurately incorporate every input's switching rates, slews and signal probabilities in deriving the EM safety of cell-internal metal segments. Additionally, we also consider the impact of EM 'recovery' on verification, which, to our knowledge, none of the state-of-the-art addresses.

In the next sections, we discuss the thought-process and analysis methodology. In particular, Section 2 discusses the prior art, Section 3 discusses the fundamental parameters affecting the reliability. The characterization methodologies are discussed in Sections 4 and 5. Section 6 describes the validation of the proposed models, while we elaborate the usage of such models in designing robust libraries in Section 7. Finally, SoC analysis and results are shared in Section 8.

2. Prior art

Aging analysis has garnered significant escalation in research community in past decade. Indeed, several tools and methods are available that analyze the circuit performance degradation caused by aging effects; both at (a) circuit level and (b) gate level. For instance, Kumar et al. [12] and Stempkovsky et al. [10] discussed the concept of transistor-level impact on gate-delay. Lu et al. [9] proposed a statistical reliability analysis method; however the transistor level details remained elusive in that. Cao et al., proposed critical-node-aware aging analysis, however, the rigor on individual transistor level details was low [7,13]; similarly for Tehranipoor et al. [8]. The work done by Lorenz et al. covers the transistor level stress in detail, however, it still did not consider the slew and frequency effects on NBTI [11]. In summary, our work advances the state-of-the-art in multiple vectors: EM verification as well as accurate aging analysis incorporating all the factors: slew, duty-cycle and frequency. It additionally incorporates accurate recovery into EM calculations, which is important from EM perspective.

3. Key parameters affecting NBTI, CHC and EM

As discussed in previous sections, the key parameters impacting the aging mechanisms can be noted as:

a. *Input slew* – at every transistor (s).
b. *Input toggle rate* – at every transistor (R).
c. *Duty cycle* – at every transistor (α).

The important thing here is the extension of above key parameters from a circuit's pin to 'every' resistor and transistor of the circuit. We note that NBTI predominantly occurs during the standby mode, while the current-driven CHC and EM mechanisms have significant impact only during the slew periods. EM, additionally, also happens during the static period of the circuit operating due to the leakage currents – as summarized in Fig. 2c. Before formulating our solution, we now study the key parameters in detail:

3.1. Parameters affecting NBTI

We use the classic R–D model for the NBTI degradation:

$$\Delta V_{thd} = \left(\frac{n^2 K_v^2 \alpha_{XM} Ct}{\zeta^2 t_{ox}^2 (1 - \alpha_{XM})} \right)^n \tag{1}$$

where the symbols have their usual meaning, [1]. In simple means, *V*th shift is proportional to the stress time as follows:

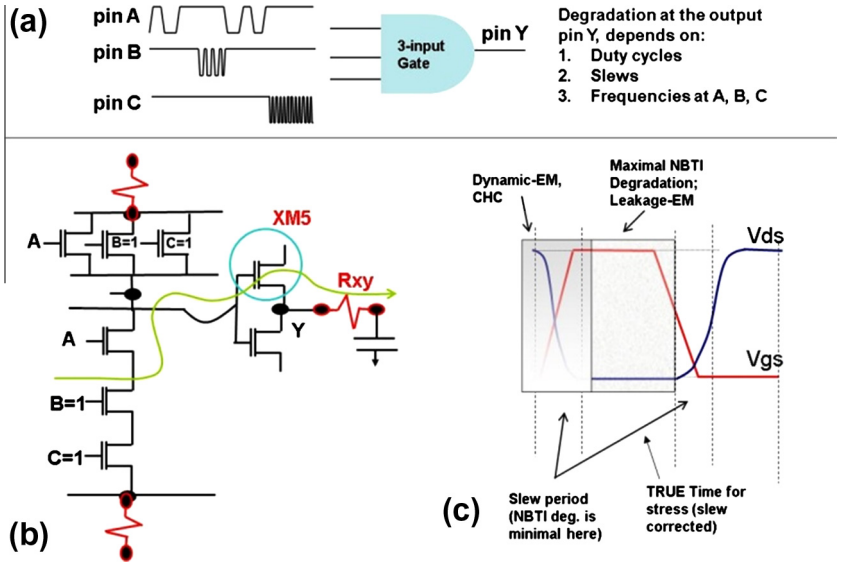

Fig. 2. (a) 3 input AND gate and its degradation scenario; (b) A-Y rising arc for the circuit, with *B*/*C* high (c) switching regimes with degradation.