Microelectronics Reliability 54 (2014) 1433–1442

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Case studies of defect localization based on software-based fault diagnosis in comparison with PEMS/OBIRCH analysis

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ARTICLE INFO

Article history:
Received 3 September 2013
Received in revised form 3 March 2014
Accepted 3 March 2014
Available online 5 April 2014

Keywords:
Software-based fault diagnosis
PEMS
OBIRCH
SCAN
SPICE
Bridge

ABSTRACT

This study verifies the accuracy of failure localization by a software-based fault diagnosis technique through comparison of the failure localization by photo emission microscope (PEMS) analysis and optical beam induced resistance change (OBIRCH) analysis. To evaluate, the software-based fault diagnosis technique was applied to 14 samples of 0.18 μm-process-node products that failed mainly due to the metal line shorts. We found that this technique was able to accurately localize the failure with a high probability (85.7%). One reason, the diagnosis returned inaccurate results is the influence of the metal line short expanding to several nets in the device simultaneously due to shorts of upper and lower metal lines. The other reason is that the fail log of the failed device itself was inaccurate due to (1) the resistance value at the short point, (2) the driving force of the cells related by the shorted points, and (3) the transition timing. We determined from our study that the rank of score calculation depends more on the mismatch rate of pass patterns than on the match rate of fail patterns. When the mismatch rate of pass patterns is less than 0.04 and the score is more than 70, the software-based fault diagnosis result is reliable. Although software-based fault diagnosis is a powerful tool for failure localization, it is necessary to combine it with hardware techniques such as PEMS analysis and OBIRCH analysis to maintain the accuracy of failure localization.

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1. Introduction

Two hardware techniques, photo emission microscopy (PEMS) analysis and optical beam induced resistance change (OBIRCH) analysis have so far been the mainstream methods of locating defects in a LSI device [1,2]. Yet, in response to the recent LSI transition towards a multilayered interconnection structure, failure localization is proving difficult using these techniques alone. Nowadays, software-based fault diagnosis is used in combination with the abovementioned techniques for this purpose. The accuracy of failure localization using software-based fault diagnosis has also been improved by new methods such as the layout-aware technique or the N-detect technique [3,4]. The accuracy of failure localization by software techniques has been fully verified with regard to stuck-at faults, but not sufficiently for the Bridge fault (the short fault) of signal lines.

In software-based fault diagnosis, the rank of score (or the match rate), which indicates the confidence of the diagnostic results is calculated from the match/mismatch rate between a simulated fail log pattern and an actual fail log pattern of a failed device. These scores have not yet been verified from a numerical viewpoint. On the other hand, hardware-based failure localization, particularly PEMS analysis and OBIRCH analysis, has already achieved high accuracy [5]. Besides, these hardware techniques are capable of detecting various defect conditions, such as the short defect, the open defect, the high resistance defect and the leak defect. The combined use of other physical analysis techniques such as the electron beam absorption current (EBAC) method and the passive voltage contrast (PVC) method increases the accuracy of fault localization as well.

In this work, we verify the fault localization accuracy of software-based fault diagnosis through comparison with highly accurate results of PEMS and OBIRCH analyses [6]. From these results, we propose a new standard "score" to indicate the confidence of software-based fault diagnosis results.

2. Experiments

The experiments were performed using a Phemos-1000 PEMS system (Hamamatsu Photonics) equipped with an InGaAs detector for photoemission analysis. The logic test pattern was looped in the AC-mode using an HCT-3000 compact tester, (Hanwa Electronics). The applied operational voltage was 1.8 V. The Phemos-1000 was

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http://dx.doi.org/10.1016/j.microrel.2014.03.002
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also used for OBIRCH analysis, where it was operated in the DC-mode with the same voltage applied as that of the PEMS analysis. For software-based fault diagnosis, we used Tessent Diagnosis (Mentor Graphics, ver. 8.2009_2.10) with the Layout-Aware Diagnostics (LAD) function to convert the failure net diagnosis (in text format) to the physical layout of the LSI device. We investigated the characteristics of the software-based fault diagnosis, the PEMS and the OBIRCH analysis results, as well as the relationships between them. For samples, we used 0.18-μm design rule 400 K-gate CMOS process logic products (5-layer metal and 1-layer polysilicon structure) with a metal line short defect due to a Via1 alignment error (Fig. 1) caused during the fabrication process. The PEMS analysis can detect the faint photon emission generated by recombined (paired) electrons and holes at a leak point of a gate oxide film, a pn junction diode, a drain avalanche hot carrier (DAHC) generated at the MOSFET drain point, and Joule heating at a metal line. On the other hand, the OBIRCH analysis can detect the faint electric current shift caused by the resistance change at a metal line short point or high resistance point and the Seebeck effect at a p or n active contact, using scanned 1300-nm infrared laser heating. As shown in Fig. 2, for a metal short point between two inverters arranged in series, the PEMS analysis detects the photon emission by Joule heating due to the electric current flow at the short point, as well as the photon emission caused by the channel hot carrier (CHC) phenomenon due to the current flowing through the MOSFET channels of the primary inverter. Furthermore, when the electric potential of the input voltage of the secondary inverter becomes intermediate due to the metal line short or open state, the DAHC photon emission is observed at the n-MOSFET drain point of the secondary inverter [7]. With the OBIRCH analysis, as stated above, the OBIRCH reaction is observed at the metal line short point, the highly resistant metal line or the p or n active contact point of the primary inverter [8]. The Me2/Via1 short point shown

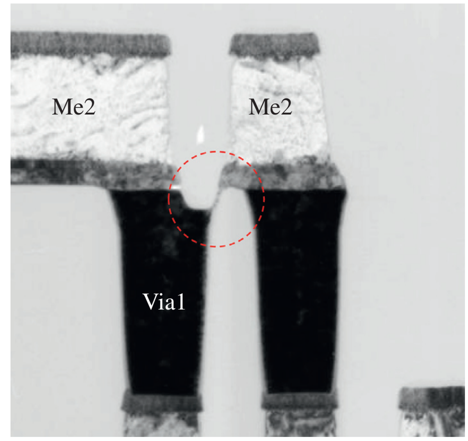

Fig. 1. Cross sectional TEM image of the Via1/Me2 short point.

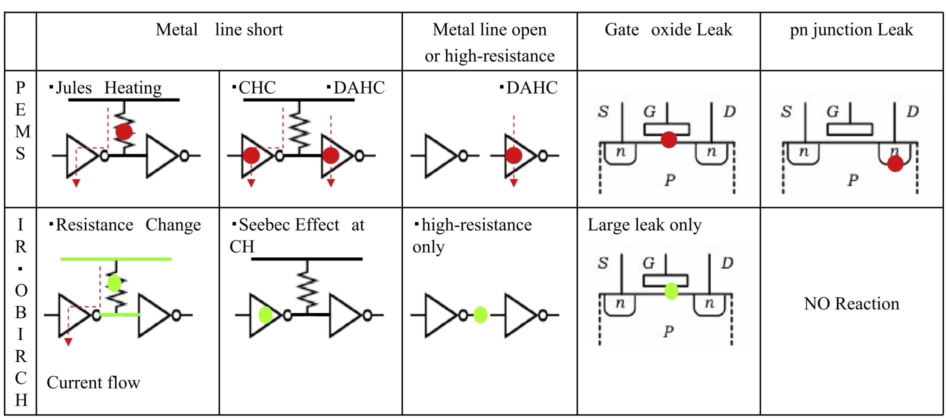

Fig. 2. Theory of emission and OBIRCH phenomena for semiconductor device failure modes.

```
symptom=1 #suspects=1 #explained_patterns=192

suspect  score fail_match pass_mismatch       type          value  pin_pathname cell_name net_pathname layout_status
------------------------------------------------------------------------------------------------
   1       100        192             0       INDETERMINATE  1     /PHYTOP/PRGBLK/PRGPGSEL/RG_ODT_regX1X/S
------------------------------------------------------------------------------------------------

BRANCH_INFORMATION
 symptom   suspect  branch  state          pin_pathname cell_name
 1              1          B1      P      /PHYTOP/PRGBLK/PRGPGSEL/RG_ODT_regX7X/S
 1              1          B2      P      /PHYTOP/PRGBLK/PRGPGSEL/RG_ODT_regX5X/S

OPEN_LOCATION
 symptom   suspect  layout_layer   category  critical_area   x_coord1    y_coord1   x_coord2   y_coord2
 1              1.2       Me1           OP        1.13E-01      1874.1400  2193.8200  1874.3800  2194.0600
 1              1.2       Me1           OP        8.10E-02      1874.1400  2194.0600  1874.3800  2194.1000
 1              1.2       Me1           OP        8.10E-02      1874.1400  2193.7800  1874.3800  2193.8200

BRIDGE_LOCATION
 symptom   suspect  layout_layer   category  critical_area     x_coord1   y_coord1   x_coord2   y_coord2
 1              1.3       Me2           S2S       1.19E-01       2708.1400  1195.9000  2708.3800  1196.1800
 1              1.3       Me2           C2C        7.46E-02      2708.1400  1195.9000  2708.3800  1195.9000
```

Fig. 3. Example of the software-based fault diagnosis: software-based failure analysis method.

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