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Review on graphene nanoribbon devices for logic applications

Juan M. Marmolejo-Tejada *, Jaime Velasco-Medina **

Bionanoelectronics Group, School of Electrical and Electronics Engineering, Universidad del Valle, Cali, Colombia, AA 25360

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ABSTRACT

Graphene nanoribbon (GNR) devices are being extensively investigated as possible candidates for replacing silicon-channel devices in the next-generation integrated circuits and systems, due to their attractive physical properties for electronic applications. This requires to implement complete models to effectively predict the electronic transport behavior of the device, which should be modeled in circuit level simulators before reaching commercial production. Different methods for electronic transport simulations in nanoelectronic devices have been studied, comprising first-principle, empirical, semi-empirical and analytical. They can be used according to the complexity of the device, and the number of atoms and inter-atomic interactions that need to be considered. This work summarizes the methods and models used to characterize and simulate nanoelectronic devices. Additionally, we review the properties of GNRs, defect issues and the most recent approaches and manufacturing techniques that could be used to design GNR-based logic circuits.

1. Introduction

The International Technology Roadmap for Semiconductors (ITRS) warn that typical horizontal dimensional scaling of complementary metal-oxide-semiconductor (CMOS) technology is reaching fundamental limits. This means that it will be impossible to continue decreasing the size of the transistors using the same technological approaches that have been used in the industry for decades. Therefore, researchers are looking for an alternative to silicon-based CMOS technology that could enable the production of smaller and faster circuits. This should make it possible to design electronic devices with more integrated functions and higher capabilities [1].

The ITRS suggests extending the functionality of CMOS integrating heterogeneous material technologies, such as germanium compounds, III–V semiconductor materials and carbon materials; implementing low-power transistors with new operating principles, such as tunneling or spin; and implementing vertical interconnections for 3D integration. This may partially or completely replace silicon in the long term (15–20 years) [2] for improving electronic systems, whose cost and performance are strongly correlated to dimensional and functional scaling (ability to improve size, power, speed or cost without loosing functionality); thus, this is likely to continue driving the semiconductor industry [1].

Graphene materials have the potential to be progressively integrated to Si devices and even replace it, in case of significantly improved performance is achieved [2]. Knowing this, recent technological roadmaps and reviews identify the properties, benefits and challenges of graphene applications for disruptive technologies [2–6]. Furthermore, the advances in the field have been highly stimulated by the increasing number of publications on graphene-related topics, patents, citations and possible applications, including energy production and storage, light-weight composites, high-speed information processing and communications, high frequency devices, high-end instrumentation, sensors and metrology, flexible electronics, transparent electrodes, photonics, biomedicine, molecular devices and spintronics, among others [2,4–8]. Consequently, the less demanding applications can be possible within the next years due to the feasibility of using lower cost and quality processes for manufacturing graphene [4].

Graphene is a 2D atomic-scale honeycomb lattice made of carbon atoms that has higher carrier mobilities than Si and other semiconducting materials (up to $10^6\,cm^2\,V^{-1}s^{-1}$ in suspended graphene [9]). However, large-area graphene is a semi-metal with zero bandgap, which causes very low on/off current ratios (I_{on}/I_{off}) when it is used as a transistor channel material in typical field-effect transistors (FETs) because the device cannot be switched off. This represents a major drawback in digital applications, since it is expected that commercial digital devices have very low leakage current when being in off state, similar to that of CMOS

* Corresponding author.
** Principal corresponding author.
E-mail addresses: juan.marmolejo@correounivalle.edu.co (J.M. Marmolejo-Tejada), jaime.velasco@correounivalle.edu.co (J. Velasco-Medina).

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technology. Consequently, one of the challenges of graphene-based devices is to reduce the off-state leakage current and improve the I_{on}/I_{off} ratios achieved so far (typically 1 or 2 orders of magnitude) for realistic applications [7].

Nonetheless, graphene can be treated to open up a useful bandgap; thus, researchers have reported the following approaches for bandgap engineering:

(i) Forming graphene nanoribbons (GNRs) by constraining large-area graphene in one dimension [10].
(ii) Biasing bilayer graphene [11,12].
(iii) Patterning graphene nanomeshes (GNMs) [13–17].
(iv) Applying strain [18,19].
(v) Applying chemical modifications to graphene [20,21].

These approaches for tuning the electronic properties of graphene for different applications and bandgap engineering have been discussed in [3,5,7].

The properties of GNRs highly depend on their size and edge shape, which can be zigzag (ZGNR) or armchair (AGNR) [10]. Since GNRs are considered periodic across their length, they are usually labeled as N-AGNR and N-ZGNR, where N is the number of carbon atoms along its width. Fig. 1 shows the atomic structure of a 10-AGNR and a 5-ZGNR.

Tight-binding (TB) calculations without spin degree of freedom show that ZGNRs and AGNRs with $N=3p+2$, where p is an integer number, are metallic, while AGNRs with $N=3p$ or $N=3p+1$ exhibit semiconducting characteristics and might be used as the channel region in FET devices [22]. However, when spin degree of freedom is included in calculations, ZGNRs have a bandgap inversely proportional to the width due to energy splitting from spin-polarized edge states [23,24]. Moreover, *ab-initio* calculations of AGNRs show that all families are semiconducting, but $N=3p+2$ has the smallest bandgap [3].

Experiments at room temperature have shown that narrow ZGNRs (less than 7-nm-wide) are antiferromagnetic semiconductors with bandgaps of ~200–300 meV, while wider ZGNRs have ferromagnetic (metallic) behavior with parallel-aligned spin states at both edges [25]. Furthermore, different processes have been used to fabricate narrow GNRs (with widths below 20 nm and down to 1.4 nm) with semiconductor properties in all cases [26–30], where GNRs with predominant zigzag edges have smaller bandgap than GNRs with similar width, but predominant armchair edges [31]. Also, researchers have probed the inverse relation between the width of the GNR and its bandgap, that is larger than 0.5 eV for the narrowest ribbons [29] and independent of crystallographic direction [26].

Similar to conventional semiconductors, it has been demonstrated that GNRs with bigger bandgaps have smaller carrier mobilities [32]. There is evidence that devices with bandgaps around 0.2–0.3 eV would require nanoribbons whose widths are less than 5 nm [22]. This constitutes a notorious disadvantage of opening a bandgap in graphene, since the carrier mobility can be reduced in more than two orders of magnitude when reaching bandgaps larger than 0.5 eV, which is required to obtain I_{on}/I_{off} ratios in the order of 10^4–10^7 [32,33]. Carrier mobility of graphene is frequently stated as its best advantage, and recent studies have demonstrated that the mobility and performance of a GNRFET device can be improved by uniformly doping the GNR, as stated in [34].

Several reviews present comprehensive summaries of graphene and GNR fabrication techniques, defects, electronic, magnetic, mechanical and optical properties, and simulation frameworks for modeling nanoelectronic devices [2,3,5–7]. This work aims to overview both experimental results and modeling approaches focused on the electronic properties of GNRs as possible candidates for digital applications.

In this context, there is an increasing interest in designing logic circuits based on GNRs; then, the main focus of this paper is to review: (i) first-principle, empirical, semi-empirical and analytical simulation methods and models of GNR-based devices, (ii) fabrication techniques and defect issues, (iii) typical and novel device structures, and (iv) logic circuits. This paper is organized as follows. In Section 2, the typical simulation methods and models are presented. Section 3 describes new fabrication techniques and device structures that may improve the performance of the devices and that could be integrated to the conventional CMOS technology. Then, approaches for functional logic gates are presented in Section 4 and perspectives for GNR-based nanodevices for logic applications in Section 5, while Section 6 presents the concluding remarks of this work.

2. Methods and models for nanoelectronic devices simulation

Compact simulation models for GNR-based devices are required to investigate the technological viability of complex ICs before reaching mass production. It is required to accurately calculate the electronic properties of graphene and other materials, depending on their different geometries, dimensions, and defects. According to the size and complexity of the system, first-principle (*ab-initio*), empirical, semi-empirical methods or analytical models can be used for simulating nanoelectronic devices, as illustrated in Table 1.

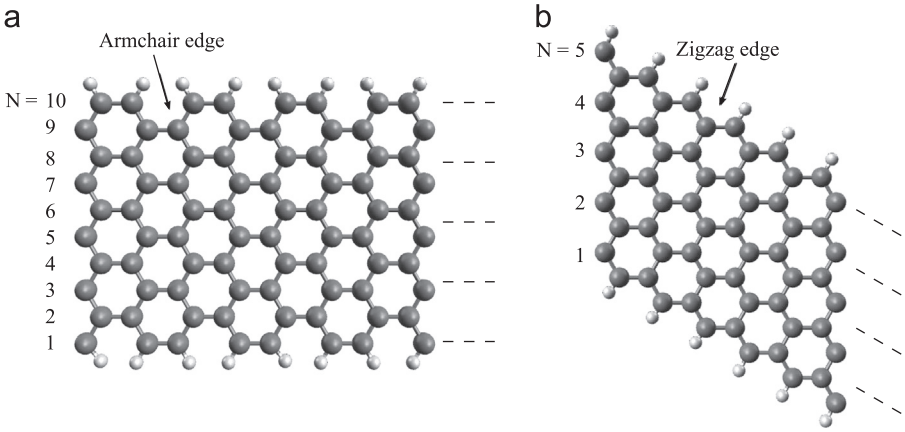

Fig. 1. Atomic structure of armchair and zigzag GNRs. (a) 10-AGNR. (b) 5-ZGNR.