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Input–output Rail-to-Rail CMOS CCII for low voltage–low power applications

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ABSTRACT

This paper presents a novel circuit design for input–output Rail-to-Rail CMOS Second Generation Current Conveyor (CCII) for low voltage and low power applications. The designed circuit is structured from a single stage Rail-to-Rail Operational Amplifier (Op-Amp) and a conventional CMOS inverter as a class AB amplifier. Therefore, it provides a high wide range for input signal and high output current driving capability operation. In this paper, a new technique for an automated design script is created to produce a constant trans-conductance (g_m) for the Rail-to-Rail Op-Amp using Open Command Environment (OCEAN) script language. The proposed Rail-to-Rail Op-Amp is based on a DC level shifter technique, which is cited at the input stage. This script allows the design problem to be cast as a program. Therefore, it offers an efficient, reliable, and fast way to implement high-performance of analog integrated circuits. Moreover, the physics-based g_m/I_D characteristic is used that is more suitable for short channel transistors in sub-micron processes. The circuit is simulated in IBM 0.13 μ CMOS technology with a single power supply 1.5-V. Virtuoso layout editor tool with caliber tools from Mentor Graphics are used to carry out the layout of the proposed circuit. The chip is fabricated by MOSIS Educational Program (MEP) and is tested to evaluate the performance of the proposed circuits. The measured and simulation results indicate a good agreement.

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1. Introduction

Recently, the research in analog integrated circuits has been become in the direction of Low Voltage–Low Power (LV–LP) design due to market requirements and advent of portable equipments such as mobile phones, laptops, hearing aids, and pacemakers [1]. Furthermore, the dramatically growth of sub-micron technology has been forced the researchers to work at low voltage supply [2]. In fact, new solutions to satisfy these strict requirements are based on both physical level (device scaling, alternate dielectric materials) and system level (new architectures, novel circuit techniques).

For the physical level, the microelectronics industry has driven transistor feature size scaling from 10 μm to 30 nm during the past 40 years. To attain a constant applied electric field, the voltage power supply should be reduced. Therefore, the low voltage circuits are necessary [3,4].

The lowering of the supply voltage produces many issues. One of the most serious issues is the Threshold Voltage (V_{TH}) of the transistor as the scaling of V_{TH} has a nonlinear behavior. Therefore, the designers have to use different and non-conventional techniques to tackle the limitation of threshold in low voltage operation.

There are many used technologies for low voltage analog circuit such as Bipolar, CMOS, Bi-CMOS [5,6] etc. The Bi-CMOS technology is limited and is not available for many designers, as they need extra process steps and high fabrication cost. On the other hand, CMOS technology is preferred as it is low fabrication cost and provides high-density area [7].

Based on CMOS technology, non-conventional techniques have been proposed to design the analog circuit for low voltage applications but the V_{TH} is still limited. One of most widely used technique for lots of low voltage applications is the Current Mode Circuit (CMC) [8]. It has some recognized advantages. The signals handled by the analog currents in their initial state as the output signals of the sensors are often currents or charges, and the signals are compressed in the entry node that allow the designer to use low voltage power supply. Moreover, this type of circuit shows a high-performance in terms of speed, bandwidth, and accuracy [9].

The CMC being up to 40 years old concept emerged as potential candidate with numerous applications in the analog field. Analog system developers welcome commercially available Current Conveyor (CC) as it provides valuable addition for the application engineer. The CC was introduced in the late sixties [10]. The original example presented by Sedra and Smith in 1968 that was

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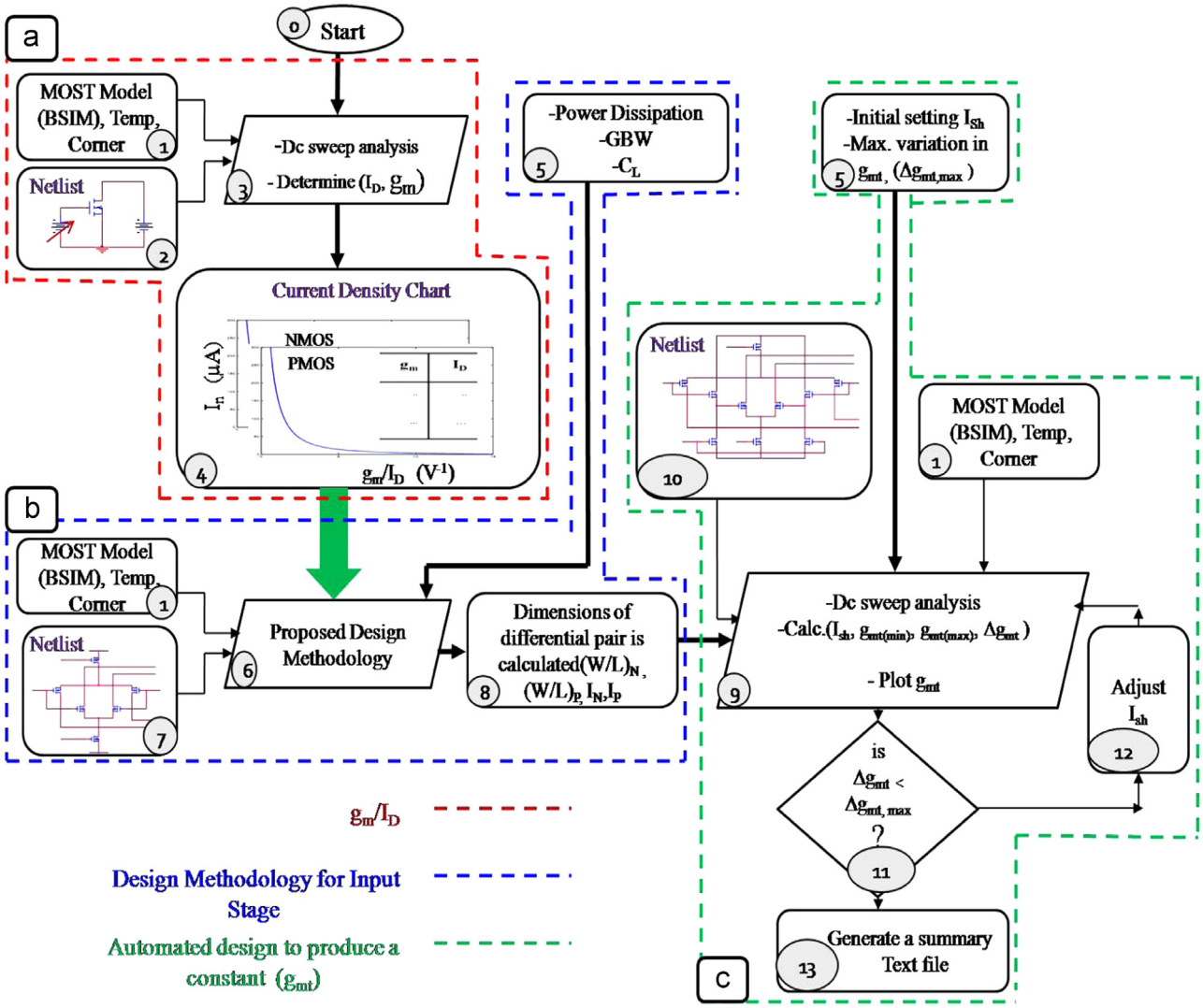

Fig. 1. Algorithm's flow chart.

generically named by the authors [11,12]. There are several schemes for the classification of current conveyor circuit such as First Generation Current Conveyor (CCI), Second Generation Current Conveyor (CCII) [13] etc. In the prior arts, many researches were carried out to prove usefulness of CCII as it has one high and one low input impedances rather than the two low input impedances of the CCI [13]. Moreover, CCII enables the designer to implement different types of current conveyor circuit such as the Third Generation of Current Conveyor (CCIII) [14].

The CCII circuit is having tremendous potential in the field of analog systems. In addition, it is a rival to voltage mode circuit due to the following reasons.

The CCII provides much better performance characteristics than Op-Amps, especially at low voltage applications. Moreover, it operates with high speed and wide bandwidth. Generally, the CCII can implement the complex analog applications. It is worth mentioning that almost all the Op-Amp circuits can be easily implemented using current conveyors such as voltage gain amplifier and voltage follower, universal filter, oscillator etc [9].

In the past, many of efforts were done to produce a LV–LP CCII based on different techniques such as Bulk-Driven Technique [15–17], Floating-Gate Approach [18–20], Class AB CCII using self cascode [21,22], Differential Pair Based Circuit, Rail-to-Rail based circuit [23–25] etc. As the matter of fact, the previous techniques suffered from some reported drawbacks [1] such as limited input and output dynamic range signals. The direction to improve the performance of CCII has been increased. Some of researchers began to create a novel structure and others combined two or more topologies to be suitable for low voltage applications [9,25].

In this paper, the input–output Rail-to-Rail CMOS CCII is presented. The proposed circuit is based on a Rail-to-Rail CMOS differential amplifier and a CMOS inverter as a class AB stage. Moreover, a novel technique for automated design for Rail-to-Rail of the Op-Amp's input stage is presented. This technique provides a constant trans-conductance (g_m) to guarantee a constant Gain Band-Width Product (GBW) value over the range of input common mode voltage. In addition, the designed circuit is fabricated and tested.

This article is organized as following; Rail-to-Rail CMOS differential amplifier with the proposed algorithm is described in Section 2. A conventional CMOS inverter is illustrated in Section 3. In Section 4, the proposed input–output Rail-to-Rail CMOS CCII is presented. The simulation and Layout results are shown in Section 5. In Section 6, tests and measurements are demonstrated. Finally, conclusion is included in Section 7.

2. Rail-to-Rail CMOS differential amplifier

As a matter of fact, there are different techniques to produce constant g_m for the Rail-to-Rail input stage but they still have a

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