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Low power and robust memory circuits with asymmetrical ground gating

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ABSTRACT

Multi-threshold CMOS (MTCMOS) technique is commonly used for suppressing leakage currents in idle circuits. The application of MTCMOS technique to static random access memory (SRAM) circuits is investigated in this paper. Two asymmetrically ground-gated MTCMOS SRAM circuits are presented for providing a low-leakage SLEEP mode with data retention capability. The read and hold static noise margins are increased by up to 7.24× and 2.39×, respectively, with the new asymmetrical SRAM cells as compared to conventional six-transistor (6T) SRAM cells in a 65 nm CMOS technology. The overall electrical quality of a memory array is enhanced by up to 103.52× and 57.75% with the proposed asymmetrically ground-gated memory cells as compared to the conventional ground-gated 6T and eight-transistor (8T) SRAM cells, respectively. The new asymmetrical SRAM cells also exhibit enhanced tolerance to process parameter variations and lower minimum applicable power supply voltages as compared with the conventional 6T and 8T SRAM cells.

1. Introduction

Leakage currents in integrated circuits are increased with CMOS technology scaling [1]. The number of transistors that are crammed onto memory banks is increased to enhance the performance and functionality of microprocessors [5–9]. SRAM arrays are therefore important sources of leakage power consumption in high performance microprocessors [5–15]. The supply voltage of integrated circuits is scaled for suppressing power consumption. The data stability and write ability of SRAM cells are however degraded with lower power supply voltage, as illustrated in Fig. 1. The shrinking dimensions of transistors and exacerbated process parameter variations aggravate the overall reliability of SRAM cells in each new technology generation [6,17–18]. Compact, robust, and energy efficient memory design is pivotal in deeply scaled CMOS integrated circuits.

Power/ground gating with a multi-threshold CMOS (MTCMOS) technology is commonly used for suppressing leakage currents in idle integrated circuits [1–4]. If the standard MTCMOS techniques (standard power-gating, standard ground-gating, or standard power&ground-gating) are directly applied to a conventional six-transistor (6T) SRAM cell, the data that is stored in the memory cell is lost when the sleep transistors are cut off to suppress the leakage currents [12,13]. Specialized power/ground gating techniques are required to maintain the data while reducing the leakage power consumption in idle memory circuits.

In this paper, two asymmetrically ground-gated SRAM circuits are presented for providing enhanced data stability during both read operations and idle status. A robust and low leakage SLEEP mode with data retention capability is provided by utilizing asymmetrical ground gating in idle memory arrays. The read and hold data stability are enhanced by up to 7.24× and 2.39×, respectively, with the new asymmetrical SRAM cells as compared to the conventional 6T memory cells in a 65 nm low power multi-threshold voltage CMOS technology. The overall electrical quality is increased by up to 103.52× and 57.75% with the new asymmetrically ground-gated SRAM circuit as compared to conventional ground-gated 6T and 8T memory arrays at the typical process corner of the 65 nm CMOS technology.

The paper is organized as follows. Previously published SRAM circuits are reviewed in Section 2. Two asymmetrically ground-gated SRAM circuits are presented in Section 3. Various memory arrays are characterized in Section 4. The impact of die-to-die and within-die process parameter variations on data stability and write ability with different SRAM cells is evaluated in Section 5. The minimum power supply voltages at which the functionality of

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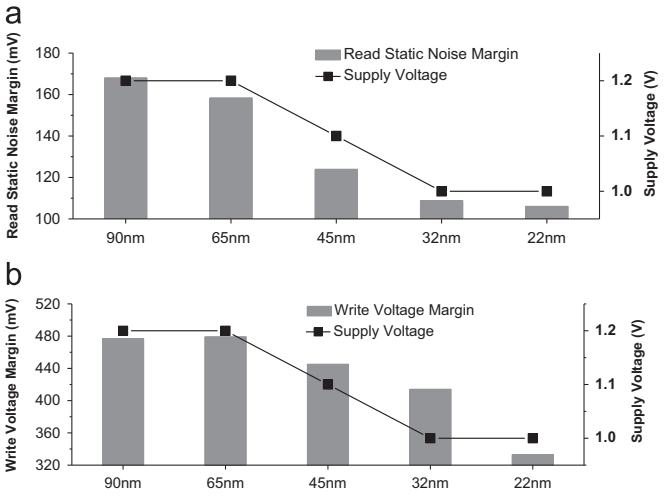

Fig. 1. The degradation of data stability and write ability of conventional 6T SRAM cells with the scaling of CMOS technology. The predictive technology models [39] are used for producing the data. The pull-up and bitline access transistors of each SRAM cell are minimum sized. $\beta=(W/L)_{\text{pull down transistor}}/(W/L)_{\text{bitline access transistor}}=3$ for each SRAM cell [12–15]. The simulation is performed with HSPICE at 90 °C. (a) Scaling of read data stability. (b) Scaling of write voltage margin.

different memory circuits can be maintained are discussed in Section 6. The paper is concluded in Section 7.

2. Conventional ground-gated SRAM circuits

Previously published SRAM circuits are reviewed in this section. A conventional ground-gated 6T SRAM circuit is presented in [7] to provide a low leakage data retention SLEEP mode. The circuit technique is illustrated in Fig. 2.

A centralized high threshold voltage (HVT) sleep transistor (N_{SL}) is used to disconnect an idle memory array (composed of conventional 6T SRAM cells) from the real ground distribution network as shown in Fig. 2. An HVT PMOS transistor (Holder) is connected in parallel with N_{SL} to implement a low leakage data retention SLEEP mode. In ACTIVE mode, N_{SL} is turned on while the Holder is cut off. The voltage on the virtual ground line (VGND) is maintained at ~0 V. The SRAM circuit thereby operates with high performance. In SLEEP mode, N_{SL} is cut off while the Holder is turned on. The voltage of the virtual ground line rises to the threshold voltage of Holder ($|V_{tp}|$). A reduced yet significant voltage difference ($V_{DD}-|V_{tp}|$) is experienced by the cross-coupled inverters in the SRAM cells. The data is maintained while the leakage currents that are produced by the idle memory array are reduced by partially collapsing the effective supply voltage of the SRAM cells.

In a conventional 6T SRAM cell, the stored data is disturbed due to the voltage division between the cross-coupled inverters and the bitline access transistors during a read operation [6–18]. The widths of the pull down transistors in cross-coupled inverters are typically tuned to tradeoff data stability, data access speed, cell area, and leakage power consumption. The data is however vulnerable to external noise even with a large β ratio due to the direct read access mechanism of a conventional 6T SRAM cell [6–15,17]. With the conventional ground-gated 6T SRAM cells, the data stability is also degraded during the low-leakage SLEEP mode due to the suppressed effective supply voltage across the cross-coupled inverters. Data stability is therefore an important concern in the conventional 6T SRAM cells.

An 8T SRAM cell is presented in [11] to enhance the data stability during read operations. The circuit technique is shown in

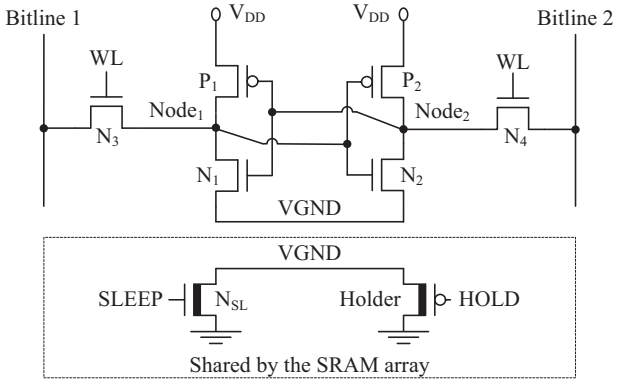

Fig. 2. A conventional ground-gated 6T SRAM circuit [7]. High threshold voltage (HVT) sleep transistors are represented with a thick line in the channel region. Different threshold voltage options are considered for the six transistors within the SRAM cells in this paper. WL: wordline. VGND: array virtual ground line.

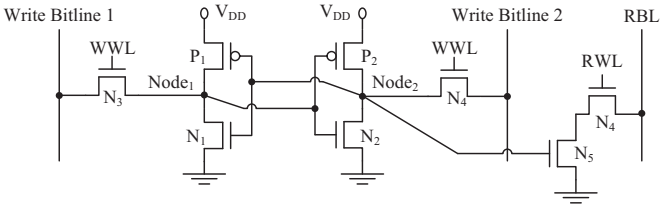

Fig. 3. A conventional 8T SRAM cell [11]. RWL: read wordline. RBL: read bitline. WWL: write wordline.

Fig. 3. As compared to the conventional 6T SRAM cells, N_4 and N_5 are added in the conventional 8T SRAM cell as separate read port. During a read operation, the read bitline (RBL) is either discharged ($Node_2$="1") or maintained at V_{DD} ($Node_2$="0") without disturbing the data that are stored in the SRAM cells. The read data stability is thereby enhanced with the conventional 8T SRAM cells as compared to the conventional 6T SRAM cells. A variety of other alternative SRAM cell topologies including different numbers of transistors are also presented to enhance the data stability, improve the write ability, and/or reduce the leakage power consumption in the previously published papers [10,14,15,22,26–36]. However, how to apply power/ground gating techniques to the conventional 8T as well as other alternative SRAM circuits to implement a low-leakage high data stability SLEEP mode is not discussed systematically in the literature.

3. Novel asymmetrically ground-gated SRAM circuits

Two new memory circuits are presented in this paper for providing a low leakage and high data stability SLEEP mode in nanoscale SRAM arrays. An asymmetrically ground-gated 8T SRAM circuit (Asym8T) is introduced in Section 3.1. A new asymmetrically ground-gated 9T SRAM circuit (Asym9T) is proposed in Section 3.2.

3.1. Asymmetrically ground-gated 8T SRAM circuit

The asymmetrically ground-gated 8T SRAM circuit (Asym8T) is shown in Fig. 4 assuming a 65 nm low power multi-threshold voltage CMOS technology. High threshold voltage (HVT, high-$|V_{th}|$), standard threshold voltage (SVT, standard-$|V_{th}|$), medium low threshold voltage (mLVT, mlow-$|V_{th}|$), and low threshold voltage (LVT, low-$|V_{th}|$) transistors are provided with the 65 nm CMOS technology that is used in this study as listed in Table 1. The Asym8T SRAM circuit has been presented in [24]. In this paper,