Microelectronics Journal 46 (2015) 1121–1128

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

Towards electro-thermo-mechanical simulation of integrated circuits in standard CAD environment

Maroua Garci *, Jean-Baptiste Kammerer, Luc Hebrard

ICube Laboratry, Université de Strasbourg-CNRS, 23 rue du Loess, 67037 Strasbourg Cedex2, France

ARTICLE INFO

Article history:
Received 12 May 2015
Received in revised form
10 September 2015
Accepted 11 September 2015
Available online 23 October 2015

Keywords:
Thermo-mechanical effects
Electro-thermo-mechanical effects
Multi-physics simulation
Integrated circuits
Direct simulation
Verilog-A

ABSTRACT

Through mechanical coupling, thermal effects can lead to drifts in circuits' electrical performances, as well as integrated circuits reliability issues. It is thus necessary to consider thermal, mechanical and electrical effects all together in a self-consistent manner. This work focuses on the electro-thermo-mechanical simulation of integrated circuits, performed in a unique Computer Aided Design environment, in the target of ICs reliability monitoring from the early design stages. An electro-thermo-mechanical simulation tool was developed using the Cadence® environment and the Spectre® simulator. The simulation principle is based on the direct approach with a mixed compact and finite element modelling. Three networks, i.e. the electrical, the thermal and the mechanical networks are automatically generated, linked together, and then simulated using a single simulator, i.e. Spectre®. The electro-thermal modelling being already developed, this paper is focused on the finite element modelling of the thermo-mechanical effects using the behavioural language Verilog-A. First simulation results on a single silicon cube have been compared with results obtained from COMSOL Multiphysics®, showing a good agreement. Finally a simplified two-material integrated circuit featuring a power device has been simulated in order to show the possibilities of the tool.

1. Introduction

The new design technologies are facing serious thermal issues resulting from the continuous increase of chip current and power densities. Failures due to electro-migration and gate-oxide breakdown, increase of delays in lines, power leakage, and thermal noise are some of critical hindrances due to high operating temperature [1–5]. Furthermore, important thermal gradients over the chip create mismatches on bias voltages and currents in analogue circuits, as well as mechanical stresses that reduce the mean time to failure of the circuit [1–3]. Indeed, different materials are used for CMOS fabrication (silicon, dielectric, metal) and for die packaging (solder, polymer…), all with different coefficients of thermal expansion (CTE) leading to thermally induced mechanical stresses when the chip is heated up [6]. Due to the piezoresistivity of silicon, mechanical stresses modify the circuit electrical characteristics. In addition, when the mechanical deformations become too strong, the system may fail [7–8]. It is thus mandatory to assess the on-chip mechanical stresses early in the design process of an integrated system.

In a previous work, an electro-thermal simulation tool using the direct approach was developed. It allows the designer for assessing the thermal effects on the electrical performances of a circuit in a standard CAD environment, i.e. Cadence® [9]. Aging models of MOSFETs that take the hot-carriers induced effect into account were also developed and electro-thermally simulated using this tool [10]. It is thus possible to determine accurately the long term behaviour of a circuit by taking thermal and aging cross-effects into account [10].

In this paper, with the ultimate aim to develop a multi-physics simulation tool of integrated circuits [11], able to take in a first time electrical, aging, thermal and mechanical effects into account, we address a new thermal cross-effect, i.e. the thermally induced mechanical stresses.

In the next section, after reminding the working principle of the electro-thermal simulation tool we have already developed, we present the way the thermo-mechanical effects can be modelled using the behavioural language Verilog-A, and how it is introduced into the existing tool in order to achieve the simulation of electro-thermo-mechanical effects in a direct approach. Section 3 presents first thermo-mechanical simulation results performed with our tool under Cadence®. The comparison with results obtained with COMSOL Multiphysics® shows a good agreement between both simulation tools. Finally the conclusion summarises our first achievement and discusses the remaining works to be

* Corresponding author.
E-mail address: maroua.garci@etu.unistra.fr (M. Garci).

http://dx.doi.org/10.1016/j.mejo.2015.09.006
0026-2692/

done in order to have a complete and efficient electro-thermo-mechanical simulator of integrated systems in a standard CAD tool such as Cadence®.

2. Electro-thermo-mechanical simulator

2.1. Direct approach for electro-thermal simulation

Electrical effects in devices, i.e. in transistors, resistors., take place locally, and the electrical potentials and currents are perfectly transferred from one point to another point in a chip thanks to metal lines. These features allow modelling the electrical behaviour of a circuit by a set of lumped device models, commonly known as the schematic of the circuit. Unlike electrical currents, heat is not conducted through well localised lines in a chip. It spreads evenly in the whole volume of the chip, and requires a Finite Element Method (FEM), or its derivatives, i.e. finite difference methods., to be modelled. The FEM modelling is generally used for its easy setup. It has the advantage to satisfy the conservation laws even with coarse approximations, and may result in high accuracy depending on the mesh fineness and the type of element, i.e. linear, quadratic... [12]. In addition, it keeps the topological information leading to a better physical insight. Indeed, depending on the type of the elements, the model results in well-known equivalent thermal networks [9,12].

To carry out an electro-thermal simulation of an integrated circuit, the circuit schematic, in which each device model may be set to different temperatures, has to be coupled to the FEM thermal model of the chip. Two approaches are used to achieve such a coupling: the relaxation method [8,13–19] and the direct method [20–27].

In the relaxation method, a thermal simulator and a conventional circuit simulator, i.e. a SPICE-like simulator, are used alternatively. A first electrical simulation is run with all devices preset at the initial temperature, i.e. the room temperature. Then, heat flux generated by each device is computed and inputted in the thermal model to compute the thermal map of the chip top face. Temperatures of all the devices, obtained from the thermal simulation, are in turn fed back to the circuit simulator, and the loop is reiterated. The relaxation between the successive electrical and thermal simulations is maintained till convergence. The method is straightforward but very fast changes cannot be considered [20] unless the simulation becomes very time consuming. It is slow because it requires data transfer and synchronization between both simulators. Worse, convergence may not be achieved in case of strong electro-thermal coupling [1].

In the direct method, both networks, i.e. the electrical schematic and the thermal network are linked in a single network through their common thermal nodes, as explained below. The resulting electro-thermal network is then simulated thanks to a conventional circuit simulator, in our case Spectre®. This direct approach is possible with modern circuit simulators which are able to solve any set of Partial Differential Equations (PDE) described in analogue behavioural languages such as Verilog-A or VHDL-AMS. Here we use Verilog-A.

As shown in Fig. 1, thanks to a script developed in SKILL®, the script language of the Cadence® environment, the FEM thermal network, which represents the silicon die and its package, is automatically generated from the analysis of the circuit layout and linked to the circuit schematic with interface entities. These bi-directional interfaces spread the heat flow coming from a device onto the corresponding device area in the thermal network, as well as compute the mean temperature of a device from all the thermal nodes of the thermal network covering the device area [9].

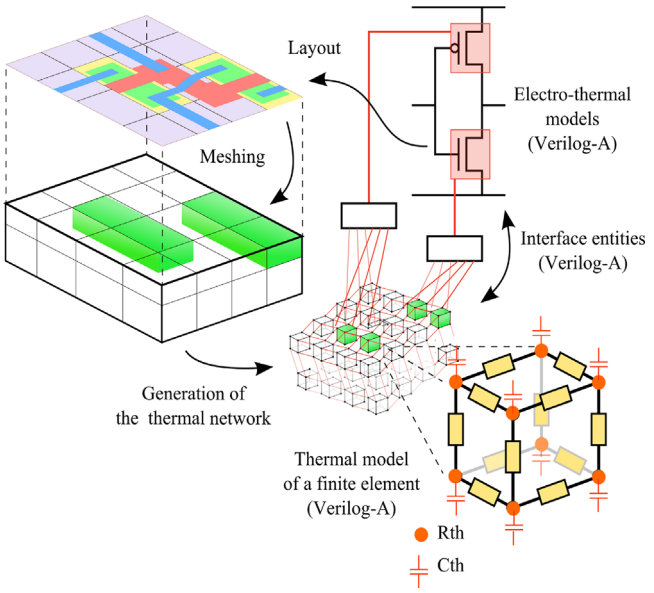

Fig. 1. Electro-thermal network generation.

The silicon die and its package are meshed by a set of parallelepiped boxes with configurable dimensions. The size of these boxes depends on the region they mesh. If they are in an area covered by a device which dissipates a high power, a fine mesh is used. Then the mesh size is relaxed when we move away from the device. Details about this multi-resolution meshing can be found in Ref. [13]. Each box represents a finite element of the material (silicon die, dielectric, package.) and is linked to the 26 boxes that represent its nearest neighbours. The heat transfer in silicon is assumed to occur by conduction and follows the well known equation:

$$\sigma_{th} \cdot \Delta T + Q = c \cdot \frac{\partial T}{\partial t} \tag{1}$$

where σ_{th} is the material thermal conductivity [W m^{-1} K^{-1}], ΔT is the temperature Laplacian, Q is the total heat generation in the material [W m^{-3}] and c is the material specific heat capacity [J m^{-3} K^{-1}]. In analogy with electricity, an elementary piece of material can be considered as a conductive element (resistor) which can store heat (capacitor). To model the thermal behaviour of a single finite element, a Cauer network is adopted. Therefore, as depicted in Fig. 1, 12 thermal resistances (R_{th}) are placed on the rectangle edges and eight capacitances (C_{th}) are connected to the rectangle vertices. Hence, R_{th} and C_{th} are expressed by the following equations:

$$R_{th} = \frac{4}{\sigma_{th}} \cdot \frac{L}{S} \qquad C_{th} = c \cdot \frac{V}{8} \tag{2}$$

where L is the box edge length, S is the corresponding box face area and V is the box volume. Each finite element can be parameterized to model any type of material (Si, SiO_2, Al, Cu.) by adapting the parameters R_{th} and C_{th}.

In the electrical schematic, the conventional compact models of the transistors, i.e. the lumped models of the circuits, are replaced by compact models which exhibit an additional thermal terminal linked to the thermal network thanks to the interface entities briefly discussed before. The temperature is thus not constant but computed thanks to the thermal network and sensed through the device additional thermal terminal. When a device dissipates electrical power, the heat it generates is directly injected into the thermal network. The time dependant temperature map of the silicon die is thus evaluated simultaneously with the electrical behaviour of the circuit schematic.