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Thermal-electronic logic circuits: Scaling down

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ABSTRACT

The thermal-electronic logic circuit (TELC) concept is a possible way to overcome the scaling down problems of the conventional CMOS integrated circuits, which have a very complex structure nowadays. The basic component of the TELC is the semiconductor–metal transition (SMT) switch, which is an extremely simple bulk type device. This work evaluates the effect of the scaling down on characteristics of the VO_2 thermal-electronic switch. Different types (lateral and vertical) of VO_2 resistors have been produced using focused ion beams and pulsed laser deposition. The measured switching time strongly correlates with the characteristic size of the device. The energy consumption (power-delay product) of the scaled-down switching device is estimated as a sum of the energy needed for heating the thermal diffusion length sized environment of the device, heating the device itself and the latent heat of phase transition of VO_2.

1. Introduction

Until now, the continuous development of electronics has been characterized by Moore's law. The scale down resulted in nano-sized CMOS integrated circuits, pushing the “red brick wall” towards the lower dimensions.

Although the current CMOS integrated circuit development is driven by a lot of innovations, there are still some limits determined by unavoidable physical effects such as tunneling of charge carriers through thin insulating regions and statistical irregularities in the number of dopant atoms.

On the other hand, there are many new ideas for building atomic or molecular scale devices for the information technology. However, there is still a gap between the up-to-date “top-down” CMOS technology and the “bottom-up” devices, i.e. molec`ular electronics, nanotubes, single electron transistors. The new thermal-electric device (phonsistor) and the CMOS compatible thermal-electric logic circuit (TELC) may help to fill this gap.

The recently proposed novel active device (phonon transistor=phonsistor) [1,2] is based on the semiconductor–metal transition (SMT) effect shown by certain materials. This effect may result in an electric resistance change in three–four orders of magnitude induced by thermal or electrical excitation.

The phonsistor is made up of only intrinsic semiconductor domains, consisting of significantly fewer regions, interfaces, and providing advanced functionality compared to a monolithic MOSFET. This way the single switches can be processed in steps that are technologically less demanding and fewer in number. The thermal-electronic logic circuit (TELC) switch can be excited by electronic and thermal signals as well, thus two different physical parameters are available for representing the different logic states.

Phase transitions involving dramatic electric changes have been investigated for the past decades. Semiconductor–metal transition (SMT; traditionally mentioned as metal–insulator transition, MIT) of vanadium dioxide (VO_2) has been known for more than 50 years [3]. Due to this special property, vanadium dioxide is investigated in a broad range of applications including switching devices [4,5], MEMS actuators [6], power limiting devices [7] and memristive elements as well [8].

In pure VO_2 the transition temperature is at about 67 °C. Above this temperature the VO_2 bulk shows metallic conductivity, while for lower temperatures it acts like an intrinsic semiconductor.

The concept of VO_2-based thermal-electronic logic devices [1] introduces a possible way to overcome silicon technology’s “red brick walls” raised by stochastic nature of semiconductor doping and the strong size limiting effect of tunneling phenomena.

2. Experimental

Two different types of samples were realized using VO_2 thin film formed with pulsed laser deposition (PLD) and focused ion beam technique: several lateral devices were constructed on

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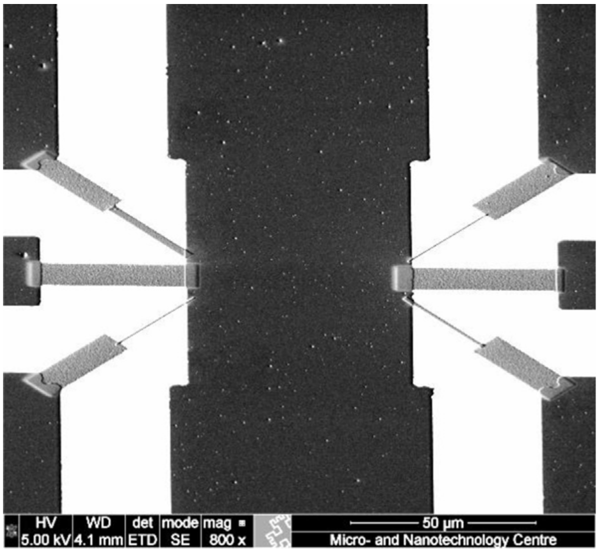

Fig. 1. SEM image of the lateral VO_2 devices. Dark gray: VO_2 thin film; white: metallization above VO_2; light gray: ablation of both thin films with laser (wide) or FIB (narrow). Active VO_2 devices were formed at the tip of each cut between the metal electrodes.

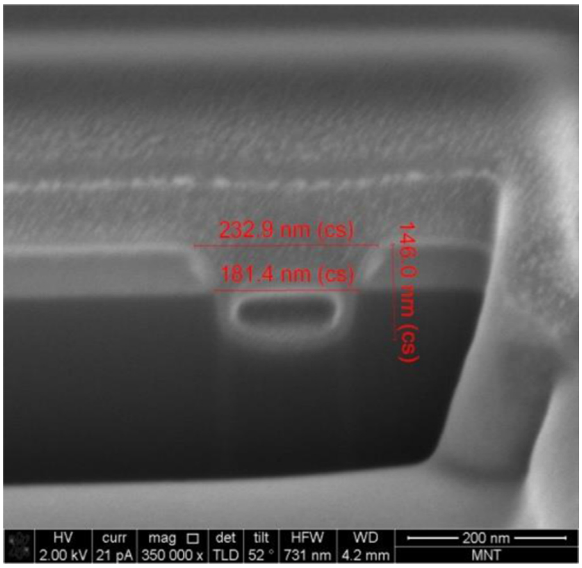

Fig. 2. Cross section SEM image of the FIB drilled hole (via, 200 nm in diameter) into SiO_2 for the vertical SMT structure. Drilling was followed by deposition of VO_2 and preparation of the metallization (top contact layer). The bottom contact was the heavily doped n^{++} Si substrate.

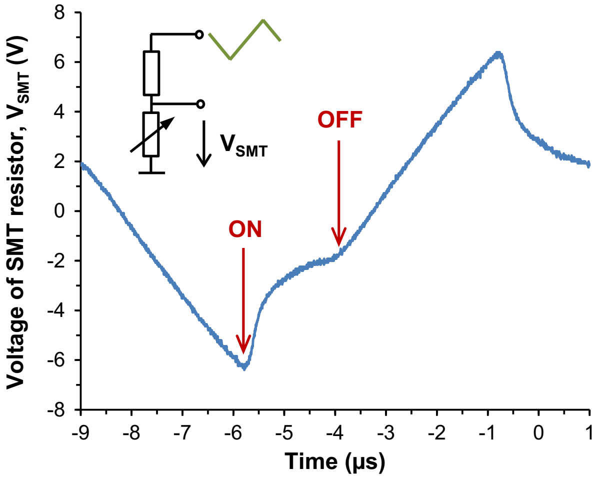

Fig. 3. Switching behavior of the µm-sized lateral SMT resistor powered by triangle voltage signal through a series resistor.

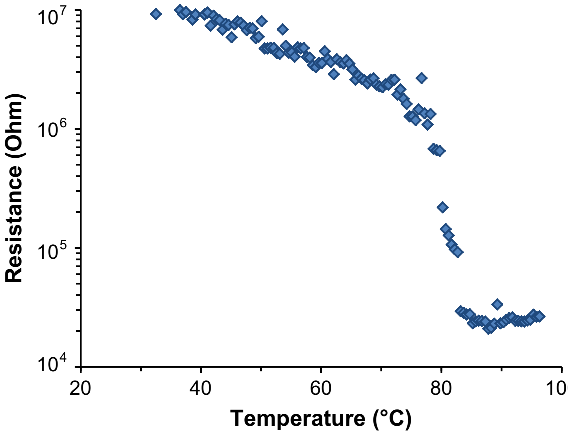

Fig. 4. Switching behavior of the nm-sized, vertical SMT resistor structure (200 nm via). Resistance abruptly decreases due to the phase transition.

sapphire substrate, designed for possibly strong thermal coupling (Fig. 1), and vertical devices were formed from VO_2 deposited into vias (200 nm to 1 µm in diameter) through SiO_2 over heavily doped Si substrate (Fig. 2) used as ground electrode.

The NAND and NOR operation of a thermal-electronic logic gate has earlier been demonstrated on thermally coupled VO_2 resistors with a characteristic size of a few tenth of mm [1]. The switching time of these devices was in the 1 s order of magnitude. In the recent work, the operation of thermally controlled VO_2 switches has been demonstrated in µm and nm scale.

In the case of µm-sized device (lateral structure, Fig. 1) the SMT resistor was powered by a triangle voltage signal through a resistor connected in series (see the inset in Fig. 3), and the voltage of the device was registered (V–t plot on Fig. 3). The deviations from the driving signal's slope and shape are caused by the switching effect, i.e. the abrupt decrease in the resistance of the device. The transition into "on" and then into "off" state is visible. The characteristic switching time of an SMT resistor is estimated to be in the magnitude of 1 µs.

In the case of a nm-sized vertical device the resistance was measured and the temperature was increased in small steps, leaving enough time for its stabilization. This way the existence of the SMT effect was clearly demonstrated (see Fig. 4).

I–*V* characteristics of this kind of vertical structure (four pieces of 1 µm diameter holes filled up with VO_2 about 80 nm in thickness, connected in parallel) are shown in Figs. 5 and 6. Using forward biasing, i.e. positive voltage on the top electrode, the thyristor-like "switch on" effect can be observed (Fig. 5). The two separate voltage drops represent the switching on of at least two resistors. However, the switching processes were irreversible; probably the high power density destroyed the devices, the platinum contact layer damage could be observed by optical microscope.

I–*V* plots using "reverse" (negative) biasing are shown in Fig. 6. at different substrate temperatures (25–80 °C). The measured current was very low in this case; probably it did not switch on the device itself by self-heating. The characteristics were still thyristor-like, considering the *I*–*V* plots between 25 and 65 °C, but the voltage peak between 0 and 1 µA was very low. The width and the level of the voltage peak were increasing with the temperature, while the resistance was gradually decreasing (see *I*–*V* slope decreasing in Fig. 6). This decrease in the resistance confirmed the