Microelectronics Journal 46 (2015) 1185–1194

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

Thermal transient measurement of insulated gate devices using the thermal properties of the channel resistance and parasitic elements

Gabor Farkas [a,*], Gergely Simon [b]

[a] Mentor Graphics, Budapest, Hungary
[b] Budapest University of Technology and Economics, Hungary

ARTICLE INFO

Article history:
Received 6 May 2015
Received in revised form
2 June 2015
Accepted 5 June 2015

Keywords:
Thermal transient measurements
Wide band gap semiconductors
Thermal standards

ABSTRACT

The paper discusses thermal transient measurements of advanced devices which operate in a temperature range where linearity cannot be assumed. However, finding a proper physical equation; valid on a wide temperature range for a device category; their calibration can be carried out at convenient temperatures. The validity of the technique can be verified by the good fit of calibrated transients at different power. Some high frequency devices have only a single known stable operation point; the validity of the measurements can be verified by comparing transients of different lengths.

In the paper measurements of a device on the R_{DSON} parameter and on reverse diode were compared. Thermal calibration of the R_{DSON} parameter of a FET gives a methodology for measuring the μ_n electron mobility.

An extension to existing transient standards is suggested. For a more accurate definition of the junction temperature a non-isothermal calculation methodology is outlined.

1. Introduction

In the previous decade a large number of new device categories have been introduced to the semiconductor market. The new devices are typically based on compound semiconductors like GaN, SiC, GaAs etc. Such devices may work at 77 K in liquid nitrogen for minimum noise; or at high temperatures up to 300 °C [1].

There exist even hybrid solutions with combining GaN on SiC and traditional Si MOSFET devices in a package; for extreme ruggedness, high voltage and low on-resistance [2,3].

HEMT devices have low R_{DSON} serial resistance and high bandwidth at cryogenic and room temperatures due to the extreme mobility of a 2D electron gas in their channel region [4].

Recently introduced Gate-Injection Transistor (GIT) devices combine the advantages of HEMTs with the optimal switching characteristics of normally off devices like enhancement MOSFETs [5].

The operational temperature range of devices is restricted in many ways. Some limitations are due to the temperature limits of die attach and package materials and these can be overridden by selecting proper ones. Some restrictions lay deeper in physics.

Semiconductor devices are formed by diffusing or implanting donor and acceptor atoms into the intrinsic crystal lattice. Normal operation can be expected when the doped regions act according to their dopant concentrations. Fig. 1 and Fig. 2 show the change of the Fermi level versus temperature in different semiconductors, governed by different concentrations of donors and acceptors. A good collection of relevant semiconductor data can be found in [6,7]. Figs. 1 and 2 are redrawn based on data of [7].

At high temperatures the semiconductor starts behaving as a piece of metal, with a conductance dictated by the temperature dependent intrinsic carrier concentration of electrons (Fig. 3). The n_i intrinsic concentration is governed by Eqs. (1) and (5), for details see [8]. At very low temperatures the $E_C=E_G-E_V$ bandgap gets wider and so threshold voltages etc. get higher which can prevent normal operation.

2. Thermal measurement standards

In the good old world life was relatively simple. Successful measurement techniques were elaborated already in the 70's [10,11]. A common feature of these techniques is that an appropriate power is to be applied on the device for a time and then its temperature is measured in a low powered state, for example when biased by a small current.

Power devices were mainly diodes or other pn structures whose V_F forward voltage shows a negative, relatively constant temperature coefficient at steady measurement current.

* Correspondence to: 1117 Gabor Denes u 2, Budapest, Hungary.
E-mail address: gabor_farkas@mentor.com (G. Farkas).

http://dx.doi.org/10.1016/j.mejo.2015.06.027
0026-2692/

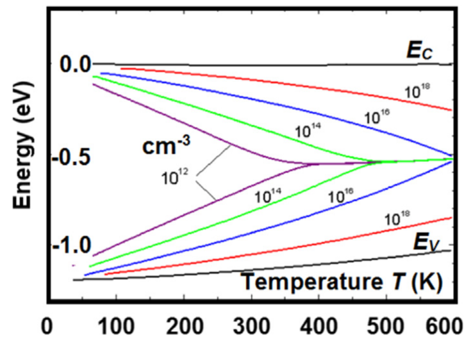

Fig. 1. Temperature change of the Fermi level for different donor and acceptor concentrations in Si.

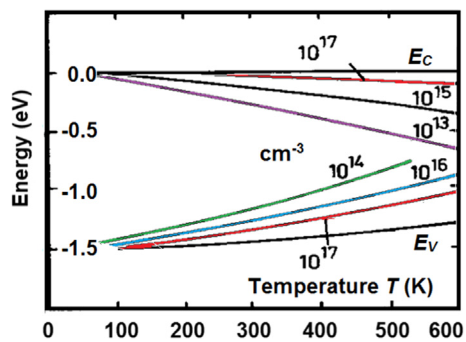

Fig. 2. Temperature change of the Fermi level for different donor and acceptor concentrations in GaAs.

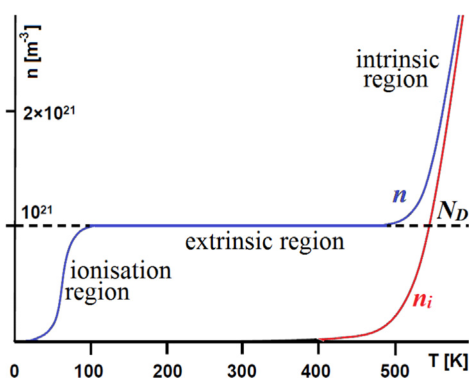

Fig. 3. Free electron concentration vs temperature in a typical semiconductor, donor concentration $N_D = 10^{21}/\text{cm}^3$.

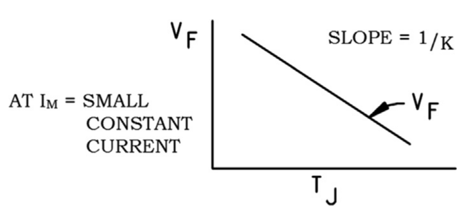

Fig. 4. Simple calibration approach of existing thermal measurement standards.

Looking a bit deeper one can find that working in a broader temperature range this linearity is far from perfect, the devices follow the Shockley model of pn junctions: $I_F = I_0\left[\exp(V_F/mV_T) - 1\right]$, where I_0 is influenced by the number a moving carriers in the semiconductor

$$I_0 \sim n_i^2 \sim T^3 \exp\left(\frac{-E_g}{kT}\right) \tag{1}$$

and such I_F has a very complex dependence on temperature. Still with silicon devices in the typical operating range of 0–120 °C the derivative

$$S_{VF} = \frac{dV_F}{dT} = \frac{\left(V_F - 3\ \text{m}V_T - \frac{Eg}{q}\right)}{T} \tag{2}$$

which yields approximately −2 mV/K in the vicinity of room temperature works well. In such a way even some contemporary standards (such as [12]) are limited to calibration instructions similar to the bit naïve approach of Fig. 4 (reworked in order to avoid copyright infringement).

Moreover, some standards define thermal resistance based on the difference of a T_J "junction" temperature and the temperature of a reference point. This latter can be, for example the ambient, package case of T_C temperature, etc. In [13,14] it has been already shown in a detailed way that package case, pins, heat sinks etc. have no single uniform temperature, definitions for thermal resistance like

$$R_{TH\_jc} = (T_J - T_C)/P$$

are oversimplified and have limited benefit when used for contemporary devices.

A deeper treatise of calibration and thermal transient measurements issues is given in [15].

It has to be noted, that the calibration of wide bandgap devices for a broad temperature range has further problems. The calibration has to span deep low and high temperatures. While in normal operation the die can be at much higher temperature than the package, which is cooled from one side, at calibration the "junction" and the calibrator thermostat are at approximately of the same temperature, which in some cases some parts of the package do not withstand.

Even the existence of a single T_J junction temperature is doubtful. In steady state the high thermal conductance of the semiconductor ensures that the spatial differences in the temperature distribution of the die are relatively small. However, thermal measurements only provide a weighted average of the steady state surface temperatures.

These facts above support that the thermal standards should be adjusted to describe properly the consequences of nonlinearities and real temperature distributions.

3. Thermal measurements on field effect devices

A bunch of the problems related to thermal measurements on field effect devices is discussed in [21] and [22].

When making the thermal characterization of FET devices; again a high power and low power state has to be defined. In case of thermal resistance measurement or thermal structure analysis a "high" power resulting in a few centigrade temperature elevation is already suitable. For reliability analysis typically higher than normal powering is used; and often current or voltage levels are also prescribed.

Typical measurement methods shown in Figs. 5–7 use the same structure as heater and a sensor, either one in the field effect

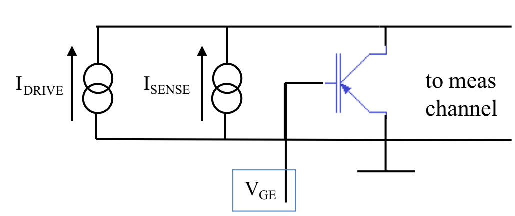

Fig. 5. MOSFET or IGBT powered and measured at constant V_{GS} voltage.