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Elimination of the effect of bottom-plate capacitors in C-2C DAC using a layout technique

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ABSTRACT

An efficient layout technique is proposed to eliminate the effect of the bottom-plate capacitors in a C-2C Digital to Analog Converter (DAC). Using this technique, the bottom-plate capacitors of 2C capacitors in the C-2C structure are placed in parallel with 1C capacitors. Then, the effect of the bottom plate capacitors is nulled by modifying the size of the main 1C capacitors. Hence, avoiding the complexity of calibration, this technique can preclude the effect of the bottom-plate to ground capacitance. Statistical simulations prove that the proposed technique is robust to non-ideal effects such as mismatch or parasitic capacitors. A 10-bit C-2C DAC is modeled in COMSOL Multiphysics using the TSMC 90 nm technology parameters to demonstrate the proposed method. Simulation results prove that the peak of INL and DNL are improved by factors of 66 and 116 compared to the conventional C-2C DAC. Moreover, using this technique multi-layer capacitors can be used along with MIM capacitors to increase the capacitance density. In a 90 nm *CMOS* technology, the area of the capacitors in a 10-bit C-2C DAC is reduced by more than 63%.

1. Introduction

Capacitive Digital to Analog Converters (CDAC) are the most popular choices compared to other types of DACs such as resistive and current-base DACs. That is because CDACs are generally low-power and the on-chip capacitors (i.e., MIM-caps) can be fabricated precisely while keeping the area occupancy reasonable. Thanks to new fabrication techniques, the matching of the MIM capacitors is more accurate than that of resistors and current sources. Moreover, capacitors are robust to environmental changes such as temperature variations.

A conventional binary weighted CDAC consumes significant amount of energy and area, especially for high resolution applications. Also, it imposes a slow step response because of the large equivalent capacitors during MSB determination in a SAR ADC. That is because the size of capacitors increase in the order of two to the power of resolution. Recently, new switching methods have been proposed to improved the power consumption. For example, the Vcm-based method [1] and the energy-efficient method [2] reduce the power consumption by 97.6% and 93.7%, respectively, for a typical 10-bit DAC. However, the large area and slow step response problems still exist. Binary weighted DAC with an attenuation capacitor at the middle of the capacitor ladder is proposed to reduce the area and power consumption and increase the speed [3]. However, it suffers from an inferior precision compared with binary weighted DACs. Step-wise charging of the DAC capacitors reduces the power consumption of every capacitive DAC at the expense of a slow switching procedure [4,5]. Other CDAC structures are proposed to reduce the area and power. In the proposed method reported in [6], a 10-bit hybrid R-C DAC is proposed which improves the static non-linearity and dynamic performance. That method improves the total area of the DAC by using resistive components. As another example, the CDAC proposed in [7] presents an ultra low-power mismatch-independent CDAC, however, it is not efficient for high resolution applications, since the CDAC employs a capacitor ladder to generate the output voltage levels.

C-2C structure was proposed to further reduce both the power consumption and the area while it improves the speed of the comparator [8]. C-2C structure is an attractive choice for SAR ADCs because of its low-power, low-area, and high-speed benefits. However, the effect of the parasitic bottom-plate capacitors deteriorates the precision of the DAC significantly which makes this structure inefficient for high resolution applications [9]. Previously reported remedies for this problem increase the complexity, area, and power consumption while they reduce the dynamic range of the DAC [9–11]. Moreover, their complexity and efficiency increase as the value of bottom-plate capacitors increase. Therefore, they are not suitable for those technologies where bottom-plate

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capacitors are more than one-tenth of the main MIM capacitors, such as thin film organic technologies (printable circuits).

This paper presents a layout technique which eliminates the effect of the bottom-plate capacitors without requiring a calibration procedure. Moreover, it reduces the total area of the C-2C DAC, since multi-layer capacitors can be used without any limiting effect on the complexity and precision of the DAC. However, multi-layer capacitors produce large bottom-plate capacitors which are not tolerable in other works because of the drawbacks of complexity, area, precision, and generally efficiency. As a result, by using the proposed technique high-resolution C-2C DACs can be designed efficiently even in thin film organic technologies in which bottom-plate capacitors are greatly larger than that in CMOS technologies.

The paper is organized as follows. Section 2 describes the effect of the bottom-plate capacitors on the precision of the C-2C DAC. Section 3 presents the proposed layout technique in detail. Also, it describes how easily multi-layer capacitors can be used while preventing the effect of the bottom-plate capacitors on precision. Section 4 presents post-layout simulation results and comparison. In Section 5, the effect of the proposed layout technique on the characteristics of the DAC is discussed. Section 6 concludes the paper.

2. The effect of the bottom-plate capacitor

A typical 5-bit single-ended C-2C structure is shown in Fig. 1 (a) in which $C2$ capacitor values are two times that of $C1$ capacitors, conventionally. If the S_1 switch at the right side of the DAC is "on" (the bolded one in Fig. 1(a)), $V_{ref}/2$ appears at the output of the DAC, since the equivalent circuit of left side is always C_u (C_{eq5}) in the C-2C structure ($C_{eq1} = \ldots = C_{eq5} = C_u$). Considering the equivalent circuit, it is noticed that C-2C structure provides the summation of descending binary fractions ($1/2, 1/4, \ldots$, and $1/2^N$) of V_{ref} at its output by connecting the V_{ref} switches. The complete description of the conventional C-2C DAC is discussed in [8]. If the bottom-plate of $C2$ capacitors are placed at the left side and the bottom-plate of $C1$ capacitors are placed at the input pins of the DAC, the equivalent circuit of Fig. 1(b) is obtained.

Taking the bottom-plate capacitors into account, we notice the considerable effect on the output voltage. The ratio of the capacitance of the bottom-plate capacitor to the MIM capacitor is referred to as γ, i.e.

$$\gamma = \frac{C_{bottom-plate}}{C_{MIM}}. \quad (1)$$

The bottom-plate capacitors of $C1$ capacitors do not affect the steady-state output voltage of the DAC. The bottom-plate capacitors of $C2$ capacitors, however, deteriorate the output voltage significantly [9]. Theory and mathematics of the effect of the bottom-plate capacitors is discussed in [9]. Here to show the significant effect of the bottom-plate capacitors on the precision, simulation results of an example are presented. Fig. 1(c) shows the INL and DNL diagram for a typical 10-bit C-2C DAC. In this figure, the bottom-plate capacitors are one-tenth of the unit capacitor (i.e., $\gamma = 0.1$). In this DAC, the DNL and INL have a peak as large as 63 LSB and 31 LSB, respectively.

The effect of the bottom-plate capacitors makes the C-2C structure impractical for high resolution data converter applications ($\geq$ 6-bit). So far, few methods are reported to decrease the error caused by the effect of the bottom-plate capacitors. Pseudo-C-2C structure is one of these methods [9]. Pseudo-C-2C method improves the precision of the DAC by resizing the $C2$ and two of the $C1$ capacitors. However, it causes a gain-error which reduces dynamic range [10]. The dynamic range reduces as γ increases.

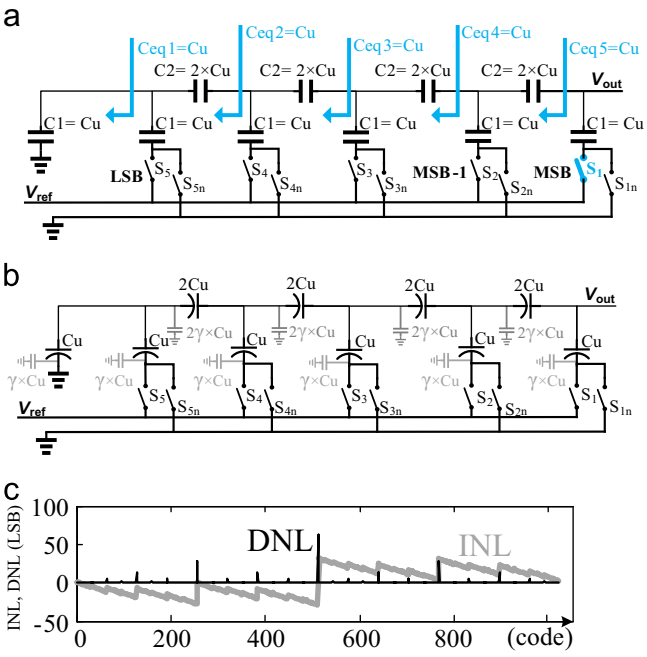

Fig. 1. (a) A 5-bit C-2C DAC, (b) bottom-plate capacitors, and (c) effect of the bottom-plate capacitors on the precision of the DAC.

Moreover, sizing the capacitors in the pseudo-method increases the area and the power consumption. For example, if the ratio of the bottom-plate capacitor over MIM-capacitor is 0.1 (i.e., $\gamma = 0.1$), the area (and almost power) is increased by 17.25% and the full scale output voltage is $0.8V_{ref}$ which means the dynamic range of the output voltage is reduced by 20%. Coarse-Radix and Fine-Radix Calibration (FRC) method (CRC and FRC) is reported as an alternative method to reduce the effect of the bottom plate capacitors [11]. Through using this method, a 7-bit C-2C DAC was achieved. However, this method increases the complexity of the circuit. Moreover, the FRC procedure needs extra control circuits and an additional DAC (a 6-bit R-2R DAC for a 7-bit C-2C DAC) to eliminate the error.

3. The proposed technique

The conceptual diagram of the proposed layout technique (neglecting the fringe capacitors) is shown in Fig. 2(b). For every $C1$–$C2$ pair of the capacitors [Fig. 2(a)], the top-plate of $C1$ is connected to the bottom-plate of $C2$ and the bottom-plate of $C1$ is connected to a metal layer beneath the bottom-plate of $C2$. Namely, $C21$ [Fig. 2(b)] is intentionally created to take the effect of the bottom plate capacitor of $C2$ under control. The equivalent circuit of Fig. 2(c) suggests that in the proposed structure, the bottom-plate capacitor of $C2$ ($C21$) is in parallel with the MIM capacitor of $C1$ (i.e., $C11$). The MIM capacitance of $C1$ (C11) is designed such that the parallel connection of $C21$ and $C11$ yields the desired ladder capacitance (i.e., $C11 + C21 = 1 \times C_{unit}$). For example, if $C21$ in Fig. 2(b) is $0.1 \times C_u$, so the MIM capacitance of C_1 capacitors are designed to be $0.9 \times C_u$. The parasitic capacitors that are connected to the input pins of the DAC are ignored because they have no effect on the steady-state output voltage of the DAC.

Practically, a metal chamber is used around $C2$ instead of a single plate. In fact, the inter-layer vias and the Metal-1 layer can be placed as a surrounding cubic chamber, as it is shown in Fig. 3. Hence, the fringe capacitors between the bottom-plate of $C2$ capacitors and the substrate can be reduced significantly. Thus, the